SECTION VIII
SERVICE

8-1. INTRODUCTION

8-2. This section provides instructions for troubleshooting and repairing the Model 83522A RF Plug-in. Information includes circuit descriptions, troubleshooting procedures, block diagrams, schematics, and component location maps for each printed circuit (PC) board assembly.

WARNING

Adjustments or repairs inside the 8350A/ 83522A with the top or bottom cover removed and the ac power connected should be avoided whenever possible. Any procedure requiring a cover to be removed from the instrument and ac power connected to the mainframe SHOULD BE PERFORMED ONLY BY QUALIFIED SERVICE PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED. With the ac power cable connected to the instrument, the ac line voltage is present on the terminals of the line power module on the rear panel and at the LINE power switch, whether the switch is ON or OFF. The ac line voltage on these terminals can, if contacted, produce fatal electrical shock. You must also be aware that capacitors inside the instrument may remain charged even though the instrument has been disconnected from its ac power source.

After you have completed a repair, check the instrument carefully to make sure all safety features are intact and functioning, and that all protective grounds are solidly connected.

8-3. SERVICE SHEETS

8-4. Each service sheet pertains to a specific assembly. Service sheets are arranged in assembly number order. Table 8-1 provides a Service Sheet Index.

8-5. Service Sheets fold out and up to facilitate access to reference material. Block diagrams appear on the fold-down apron. Component location maps, PC board pin-edge connections, and pertinent circuit information (e.g., waveforms) are found on the fold-up apron of the service sheet, with the schematic directly below. A circuit description with assembly level troubleshooting is located on the pages immediately preceding the service sheet.

8-6. SCHEMATIC DIAGRAM NOTES

8-7. Figure 8-1, Schematic Diagram Notes, provides definitions to schematic symbols.

8-8. MNEMONICS

8-9. Table 8-13 alphabetically lists and defines all 83522A signal mnemonics, references the point-to-point distribution of each signal to and from the PC board sockets and the cable connectors on the A10 Motherboard assembly, and identifies the signal source. This table is located on the A10 Service Sheet.

8-10. SERVICE AIDS

8-11. Two Extender Cable Assemblies, HP Part Number 08350-60034 (64 pin) and 08350-60035 (17 pin), are designed to power the RF Plug-in when it is removed from the 8350A Sweep Oscillator for troubleshooting. These service aids are recommended for convenience in servicing the 83522A.

8-12. A 44-pin extender board (HP Part No. 08350-60031) is available to allow access to printed circuit board assembly components while maintaining electrical contact with the plug-in. This and other service aids are referenced in Section I, Table 1-3, of this manual.

Table 8-1. Index of Service Sheets

BASIC COMPONENT SYMBOLOGY

R, L, C	Resistance is in ohms, inductance is in microhenries, capacitance is in microfarads, unless otherwise noted.
P/O	Part of.
*	Indicates a factory selected component.
	Panel Control.
	Screwdriver adjustment.
	Encloses front panel designation.
	Encloses rear panel designation.
	Circuit assembly borderline.
	Other assembly borderline.
	Heavy line with arrows indicates path and direction of main signal.
	Indicates path and direction of main feedback.
	Earth ground symbol.
	Assembly ground. May be accompanied by a number or letter to specify a particular ground.
	Chassis ground.
n	Represents n number of transmission paths.
	Test Point: Terminal provided for test probe.
	Pin Edge Connector output of PC board.
(**)	Indicates wire or cable color code. Color code same as resistor color code. First number indicates base color, second and third numbers indicate colored stripes.
	Indicates shielding conductor for cables.
	Indicates a plug-in connection.
	Indicates a soldered or mechanical connection.
	Connection symbol indicating a male connection.
	Connection symbol indicating a female connection.
	Resistor.
	Variable Resistor.
	General purpose diode.
	Step recovery diode.
	Schottky diode.
	Breakdown Diode: Zener
	Light-Emitting Diode.
	SCR (Silicon Controlled Rectifier).
	FET: Field Effect Transistor (N-channel).
	FET: Field Effect Transistor-Guarded gate (N channel).
	Dual Transistor.
	Transistor NPN
	Transistor PNP
	Electrolytic Capacitor.
	Toroid: Magnetic core inductor.
	Operational Amplifier.
	Fuse
	Pushbutton Switch.
	Toggle Switch.
	Thermal Switch.
Σ	Summing Point.
	Oscillator; RPG (Rotary Pulse Generator).
BI	Fan, Motor.
	Toroidal Transformer

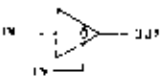
LOGIC SYMBOLOGY

&	AND Gate
≥1	OR Gate
&	NAND Gate
≥1	NOR Gate
=1	Exclusive OR Gate
	Buffer/Amplifier
	Inverter
	Negation symbol. Line is active low.
	Indicated edge-sensitive input.

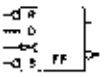
Figure 8-1. Schematic Diagram Notes (1 of 3)

INTEGRATED CIRCUIT SYMBOLOGY

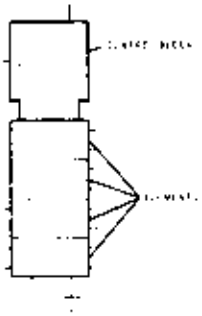
Schmitt Trigger: The gate of the Schmitt Trigger switches at different points for positive- and negative-going signals. The difference between the positive and negative thresholds is defined as hysteresis voltage.



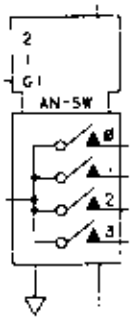
3-State Buffer: Three States:
Enable (EN) Input low: High impedence output.
Enable input high: Output = 0 or Output = 1



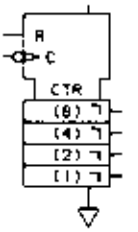
Data Flip-Flop: Set (S) and Reset (R) are asynchronous controls. Active S sets the noninverting output high and the inverting output (○—) low; active R resets both outputs. When S and R are both inactive, the outputs remain latched in the last state. An active clock (—▷) enables the D input, at which time the noninverting output = D, and the inverting output = $\bar{D}$.



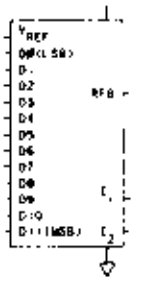
Control Block: All controlling inputs (gates, clocks, inhibits, etc.) connect to the control block.
Elements: Can be one or more of any logic function (flip-flop, counter, gate, RAM, etc.). Data inputs are on the left side of element, data outputs on the right.



Analog Switch: Control lines 1 and 2 decode to select one of four inputs. G1, high=enable.



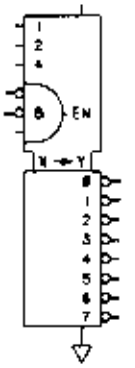
Counter: Binary-weighted registers count on the falling edge of each clock pulse. Active (high) R clears all registers.



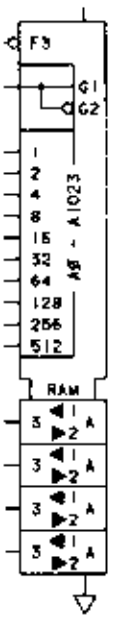
Digital to Analog Converter (DAC): Provides a scaled current output (I_1), the product of V_{REF} and the fractional binary input:

$$D_{11}2^{-1} + D_{10}2^{-2} + D_9 2^{-3} + \ldots D_0 2^{-12}$$

The product of V_{REF} and complement of the binary input appears at I_2.



Decoder: The logic states of the three select lines A, B, and C, and the three enable inputs (EN), determine which one of the eight outputs will be decoded. The selected output will be low, while all others are high.



Random-Access Memory (RAM): Binary addresses (A0 to A9) access one of 1024 registers in RAM. When G1 is high, bits appearing at D0 to D3 will be written to the addressed location (A0 to A9). When G2 is low, bits appearing at D0 to D3 have been accessed from the addressed location.

Figure 8-1. Schematic Diagram Notes (2 of 3)

FUNCTION LABEL ABBREVIATIONS

Σ	Adder	◇	Open Collector	LED	Light-Emitting Diode
	Amplifier/Buffer		Monostable Multivibrator	MUX	Multiplexer
	Schmitt Trigger	BCD	Binary Coded Decimal	RAM	Random-Access Memory
&	AND	CTR	Counter	REG	Register
≥1	OR	DAC	Digital-to-Analog Converter	ROM	Read Only Memory
=1	Exclusive OR	FF	Flip-Flop	RPG	Rotary Pulse Generator
X→Y	Encoder, Decoder	I/O	Input/Output		

LINE LABEL ABBREVIATIONS

CK, C	Clock Input	MSB	Most Significant Bit	T	Trigger Input (Monostable)
D	Data or Delay Input (Flip-Flop)	Q	Output	WR	Write
EN	Enable	$\bar{Q}$	Not Q Complement of Q	+1	Count Up
F	3-State Enable Input	R	Reset or Clear Input	−1	Count Down
G	Gating Input	RD	Read	3-ST	3-State (placed by function)
LSB	Least Significant Bit	S	Set Input		

Figure 8-1. Schematic Diagram Notes (3 of 3)

8-13. TROUBLESHOOTING

CAUTION

Improper methods of discharging the −40 Volt supply may result in damage to the instrument. Refer to the 8350A Sweep Oscillator Operating and Service Manual for these procedures.

8-14. Troubleshooting is generally divided into two maintenance levels in this manual. The first level isolates the problem to a circuit or assembly. SELF-TEST (described in paragraph 8-16) together with the Overall Block Diagram and Troubleshooting hints, helps to isolate the problem source to a particular assembly.

8-15. The second maintenance level isolates the trouble to the component. Operator-initiated tests, schematic diagrams, and circuit descriptions for each assembly aid in troubleshooting to the component level.

8-16. SELF-TEST

8-17. 8350A software provides microprocessor and operator-initiated checks. These checks verify the proper functioning of the majority of the 8350A and 83522A digital circuitry and a portion of the analog devices.

8-18. Whenever the 8350A is powered ON, or the front panel **INSTR PRESET** pushbutton is pressed, instrument SELF-TEST is initiated. Instrument SELF-TEST checks a number of circuits in both the 8350A and the 83522A. If a failure in the 83522A is detected during SELF-TEST, error code E001 will be displayed. Table 8-2 lists other error codes associated with the 83522A RF Plug-in.

8-19. If the front panel displays an error code, refer to the Overall Block Diagram and Troubleshooting section. This section will help the operator to define the problem area.

8-20. OPERATOR-INITIATED TESTS

8-21. The 8350A microprocessor services several operator-initiated tests of the 83522A to check functions which are not exercised during SELF-TEST. The tests may be initiated by making the appropriate key entry indexed in Table 8-3.

8-22. Access to most of the 83522A digital circuitry can be achieved through local programming with the following key entry commands:

Function	Key Entry
Hex Address Entry	SHIFT 0 0 M1 * (enter hex address)
Hex Data WRITE	M2 (enter data: two hex digits)
Hex Data READ	M3
Hex Data Rotation Write	M4
Hex Address Fast Read	M5

*To address a different location, press M1 and enter the new address, or use the increment or decrement keys ◆ ◆ to step to the new address.

Table 8-2. Error Codes Associated With 83522A

Error Code	Circuit Tested
E001	Addresses 83522A ROM and reads Check Sum back to 8350A.
E050	Erroneous Front Panel Pushbutton Flag.
E051	Erroneous Front Panel Pushbutton Code received by 8350A Microprocessor.
E052	Checks for Timer failure in A3.
E053	Checks PIA circuits in A3.

NOTE

Error codes E050 through E099 are reserved for the RF Plug-ins however, not all are used.

Table 8-3. Operator Initiated Self Test Routines Available

Data Entry	Test	Assembly*	Test Point for Waveform
SHIFT 50	Power Level DAC	A4	A4TP2
SHIFT 51	Power Sweep DAC	A5	A5TP8
SHIFT 52	Scale/Offset DACs	A6	A6TP1/A6TP2
SHIFT 53	Address Decoder; checks major address decoder lines	A3	A3U6, A3U7, A3U9, A3U13
SHIFT 54	Address Decoder; checks individual board address decoders	A4, A5, A6, A7, A8†	Address Decoders
SHIFT 55	Interrupt Control	A3	A3U4-38

*Refer to troubleshooting procedure of the appropriate assembly for waveforms and detailed procedures.
†The address decoder for the A8 Sampler is on the A7 Marker Assembly.

By entering the Hex address location of a specific device, that device can be exercised. (Addresses are supplied next to the mnemonic on each schematic. Also, circuit descriptions usually include Address Decoder Tables to define the addresses used on that particular assembly.) A hex address entry must be made prior to any of the following:

NOTE

Before addressing an 83522A component, determine whether or not the 8350A microprocessor can READ or WRITE to that particular device. The majority of 83522A digital integrated circuits do NOT have both READ and WRITE capabilities.

- HEX DATA WRITE. M2 . allows the operator to write any combination of hex data bytes to the addressed device. The outputs can then be checked to see if the device is functioning properly.

- HEX DATA READ. M3 . allows the operator to read the outputs of an addressed device.

- HEX DATA ROTATION WRITE. M4 . strobes a '1' (high state) through a column of zeroes (low states) to the addressed device. In effect, Hex Data Rotation Write is a rapid WRITE mode, exercising the addressed device in real time. The microprocessor inputs the data continuously, without servicing interrupts from the rest of the instrument. Latch enable lines, inputs, and outputs can be checked in this mode. Figure 8-2 illustrates the appropriate waveforms.

- HEX ADDRESSED FAST READ. M5 . provides an operator-initiated check for verification of the data bus, in which the addressed device is clocked in real time. Latch outputs can be traced from the onboard location back throuh the data bus to the microprocessor. At each buffer, verify TTL level response to the enable pulse. Enable line waveforms are shown in Figure 8-3.

8-23. HEXADECIMAL

8-24. Hexadecimal is the number system used to locally address the 8350A and 83522A logic components. Available operator initiated self test routines are indexed in Table 8-3.

8-25. The hexadecimal system uses 16 digits: 0 through 9 and A through F. Since 16 is the fourth power of two, four-bit binary numbers can be expressed with one hexadecimal digit, making local programming easier. Table 8-4 provides hexadecimal conversions to binary and decimal equivalents.

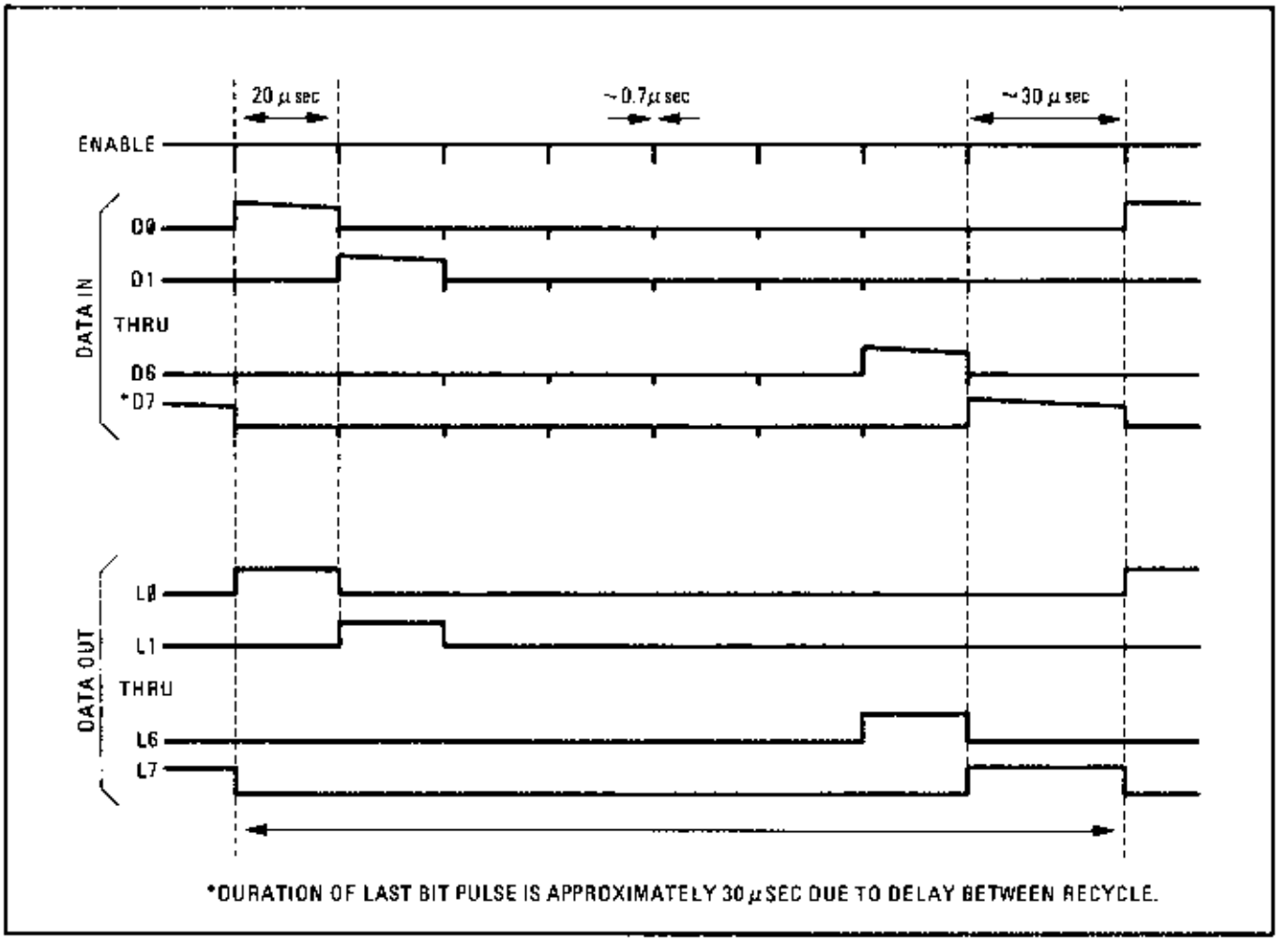


Figure 8-2. Hex Data Rotation Write — Bit Pattern

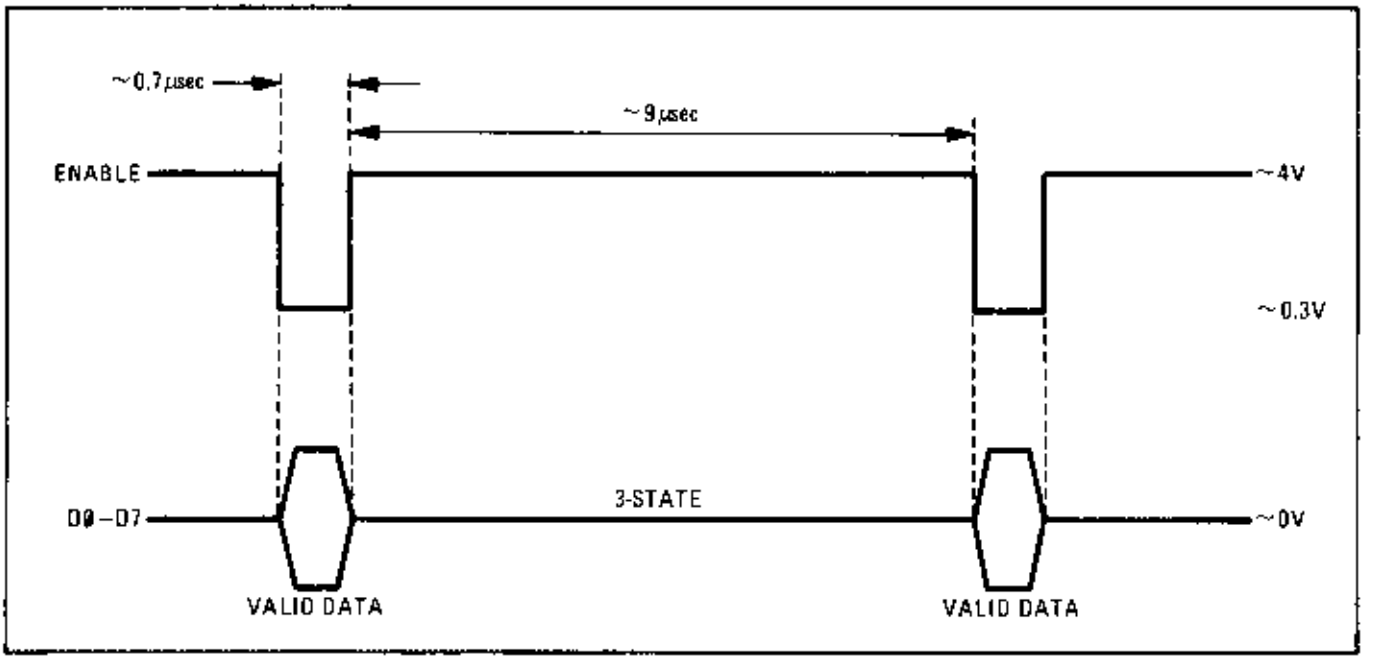


Figure 8-3. Hex Addressed Fast Read — Timing Diagram

Table 8-4. Hexadecimal Equivalents

Hexidecimal	Binary	Decimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
A	1010	10
b	1011	11
C	1100	12
d	1101	13
E	1110	14
F	1111	15

8-26. When the 8350A is in the Hex Data WRITE mode (refer to paragraph 8-22), several front panel keyboard pushbuttons function as hexadecimal digits. Figure 8-4 illustrates the DATA ENTRY keyboard with the hexadecimal digits assigned to each pushbutton.

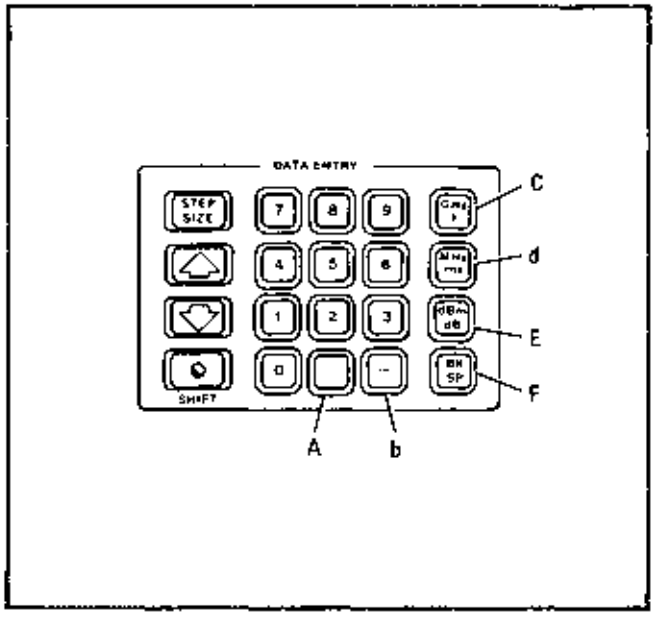


Figure 8-4. Hex Entry Keys

8-27. RECOMMENDED TEST EQUIPMENT

8-28. Test equipment required to maintain the Model 83522A is listed in Section I. If the equipment listed is not available, equipment that meets the minimum specifications shown may be substituted.

8-29. REPAIR

8-30. Module Exchange Program

8-31. This instrument may be quickly repaired by replacing a defective module with a restored-exchange module. To support the module repair concept, Hewlett-Packard has set up a module exchange program.

8-32. The procedure for using the module exchange program is given in Figure 8-5. When you locate the defective module, order a replacement module through the nearest Hewlett-Packard sales office. The restored-exchange module will be sent immediately directly from a customer service replacement parts center. When you receive the exchange module, return the defective module in the same special carton in which the exchange module was received. DO NOT return a defective module to Hewlett-Packard until you receive the exchange module.

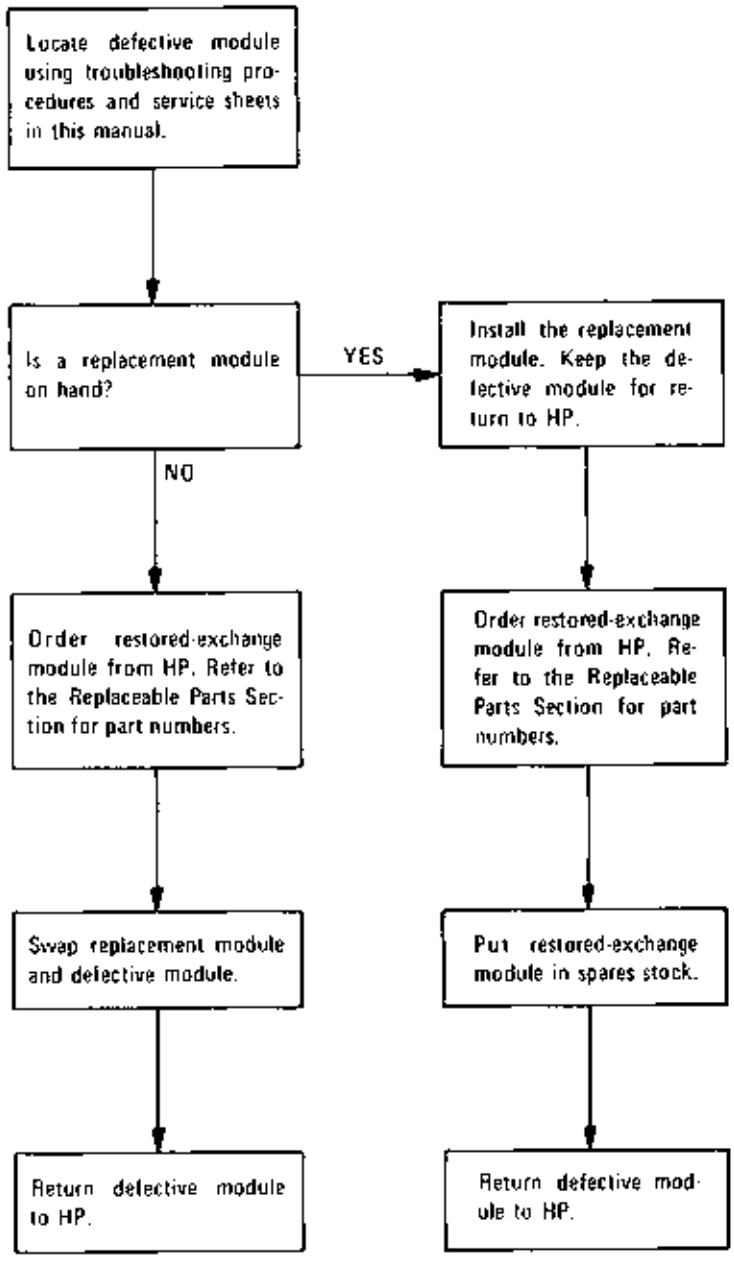
8-33. If you are not going to return the defective module to Hewlett-Packard, or if you are ordering a module for spare parts stock, etc., order a new module using the new module part number listed in Table 6-3.

8-34. The Hewlett-Packard module exchange program allows you to obtain a fully tested and guaranteed restored-exchange module at a reduced price. (The reduced price is contingent upon return of the defective module to Hewlett-Packard.) Assemblies available for module exchange are listed in Table 6-1.

8-35. Replacing YIG Oscillator A12 or YO Driver A6

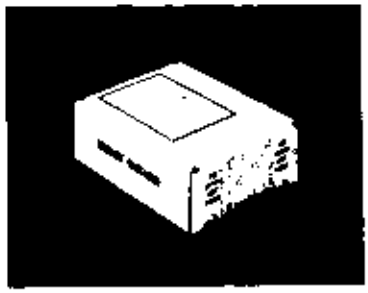
8-36. Each YIG Oscillator requires a unique set of six resistors to be installed in YO Driver A6 for proper YIG coil drive. The value of these resistors is documented on a label attached to the side of the 83522A near the RF section. If A6 is replaced, these six resistors (A6R1, A6R3, A6R38, A6R39, A6R40, and A6R41) must be removed from the old board and installed on the new board. Also, if YIG Oscillator A12 is replaced, the six new resistors shipped with the

The module exchange program described here is a fast, efficient, economical method of keeping your Hewlett-Packard instrument in service.



*HP pays postage on boxes mailed in U.S.A.

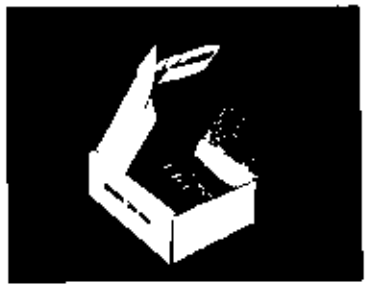
A.



Restored-exchange modules are shipped individually in boxes like this. In addition to the circuit module, the box contains:

Module repair report
Return address label
Tape for resealing box

B.



Open box carefully - it will be used to return defective module to HP. Complete repair report. Place it and defective module in box. Be sure to remove enclosed return address label.

C.

Seal box with tape provided. Inside U.S.A.*, stick preprinted return address label over label already on box, and return box to HP. Outside U.S.A., do not use address label instead, address box to the nearest HP office.

Figure 8-5. Module Exchange Procedure

oscillator must be installed on A6 in place of the old resistors. (In some cases, some of the resistors may be deleted, depending on the drive requirements of the individual oscillator.)

8-37. Rear Panel Connector Replacement

8-38. When replacing rear panel connector P1, connector P2 also must be partially removed to remove P1 from the rear panel casting.

8-39. When reassembling rear panel connectors P1 and P2 into the casting, alignment is very critical to ensure proper interface with the mating 8350A connectors. Align the center of the attaching bolts with a steel rule and tighten in place in accordance with the placement drawing in Figure 8-6.

8-40. AFTER-SERVICE PRODUCT SAFETY CHECKS

8-41. Visually inspect the interior of the instrument for any signs of abnormal internally generated heat, such as discolored printed circuit boards or components, damaged insulation, or evidence of arcing. Determine and remedy the cause of any such condition.

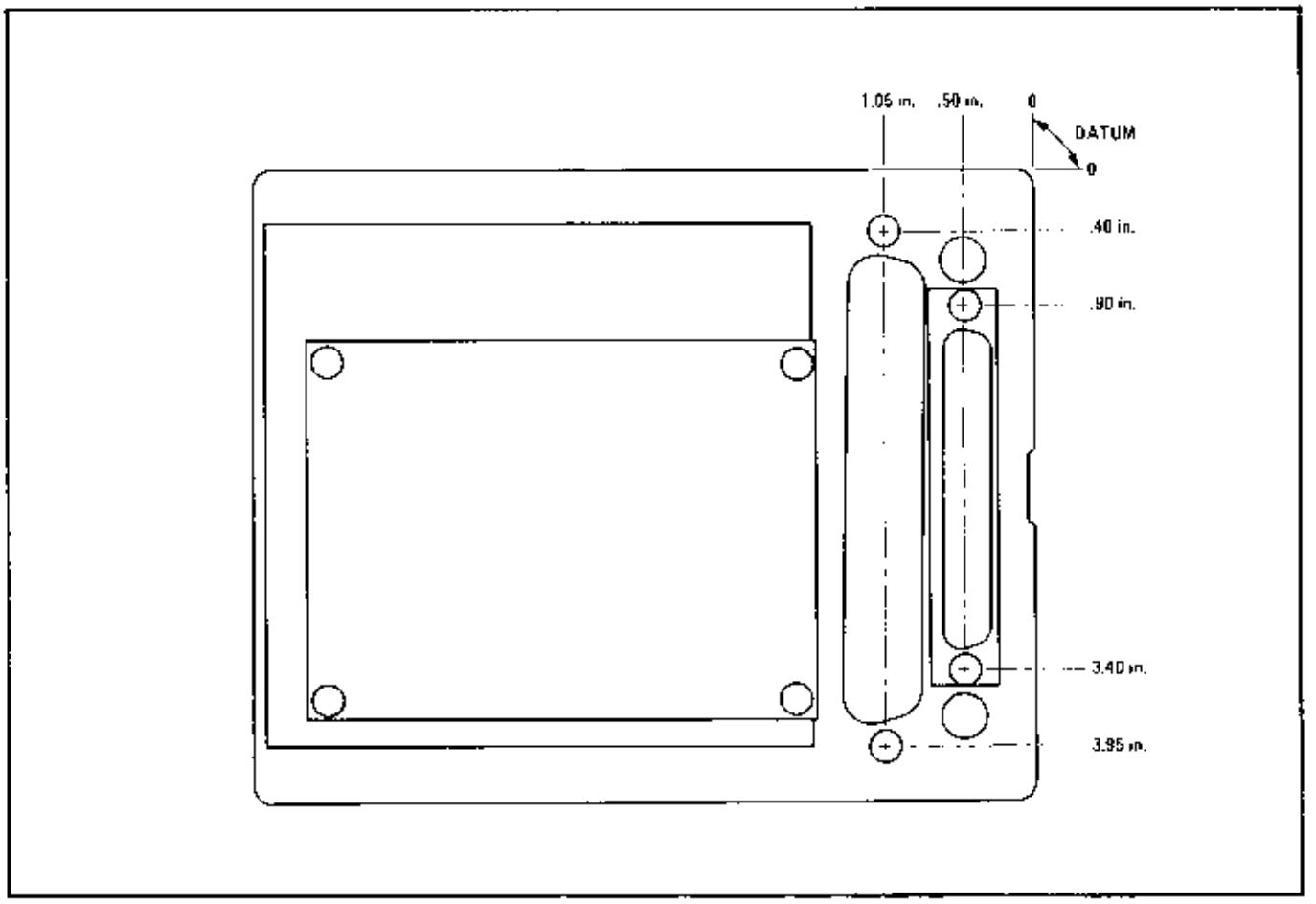


Figure 8-6. Rear Panel Connector Alignment Diagram

83522A RF PLUG-IN SIMPLIFIED BLOCK DIAGRAM DESCRIPTION

The operating principles of the 83522A RF Plug-in are described in two levels. The Functional Block Diagram Description describes major functional areas of the instrument. The Troubleshooting Block Diagram Description discusses the theory in greater depth, and outlines the breakdown of functions among the various instrument assemblies.

FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

The HP Model 83522A RF Plug-In, used with the 8350A Sweep Oscillator, covers the 0.01 to 2.4 GHz frequency range with +13 dBm of leveled RF power. Internal crystal markers, at 1, 10, or 50 MHz intervals, are available to produce Z-axis intensity markers or 1 dB amplitude markers up to 2.4 GHz (below 1 Ghz for the 1 MHz markers). In addition to internal leveling, external detectors or power meters can be used to level the RF power. Furthermore, the 83522A can sweep power proportional to either frequency or sweep.

The 83522A can be broken down into five functional sections:

- Digital Control and Front Panel
- Frequency Control
- Power Control (ALC)
- Marker Generation
- RF Section

The functional description for each of these five functions is described briefly below.

Digital Control/Front Panel

The entire 83522A is digitally controlled by a microprocessor in the Model 8350A. It must be emphasized that nearly all functions are commanded by the 8350A: very few activities take place without microprocessor intervention.

The Digital Control section of the 83522A is the focal point of all communication between plug-in and 8350A. It receives commands ordered by the microprocessor along the 8350A's instrument bus. Once in the 83522A, these commands are decoded and routed to the appropriate part of the plug-in to control virtually every capability. The Digital Control section also contains a block of Read Only Memory (ROM), which provides the microprocessor with the constants and program software tailored to the plug-in. The Digital Control section, then, is the "control center" for the entire plug-in.

The Front Panel Interface is the communication link between the Front Panel displays or controls and, via the 8350A microprocessor, the rest of the plug-in. It receives and stores information to be presented by the numerical display or annunciators through the Digital Control block, and continuously refreshes the display. It also receives the user's commands through the Front Panel pushbuttons and Rotary Pulse Generator (RPG), and sends them back through the Digital Control block to the 8350A microprocessor. Certain analog signals, such as FREQ CAL, pass through the Front Panel Interface to the appropriate part of the 83522A.

Frequency Control

The Frequency Control block is responsible for converting the tuning ramp (VTUNE) from the 8350A Sweep Oscillator into a drive current controlling the YIG Oscillator (YO) frequency. The tuning voltage is digitally scaled and offset to yield a voltage proportional to the YO's frequency. A delay compensation signal is summed in with the scaled tuning voltage to compensate for response delays in the YO. Lastly, low-frequency components of external frequency modulation (FM) are filtered and also summed in to produce a total YO control voltage. However, the YO is current controlled, so a Current Driver converts the control voltage to a drive current for the YIG Oscillator.

The high-frequency FM components cannot be summed in with the drive current due to the limited dynamic response of the YO's main tuning coil. Instead, they are filtered off and sent to a separate coil built into the YO to allow smaller but faster frequency modulation.

The Sweep Interrupt block, used in other multiband RF plug-ins, monitors the tuning voltage (VTUNE) when the RF plug-in is performing a sweep requiring multiple bands. When a tuning voltage corresponding to the end of the band is sensed, these circuits temporarily stop the sweep ramp and interrupt the 8350A microprocessor. The microprocessor then prepares the plug-in for the new band, including new scaling and offset values, and continues the sweep. This portion of the frequency control circits is not used in the 83522A.

Power Leveling (ALC)

The Power Control circuits determine the RF output power level, and ensure that the power is constant across the sweep. A feedback loop detects the RF power level, compares it with a reference voltage, and adjusts a PIN modulator in the RF path to correct for amplitude errors.

The power level is digitally programmed from the 8350A Sweep Oscillator. A scaled sweep ramp to provide the power slope or power sweep function is added, yielding a reference power level.

An RF detector provides a voltage proportional to the actual RF power level. This is then compared to the desired reference power level voltage to produce an error voltage. The error is then amplified to drive a PIN modulator and correct the output power level.

Marker Generation

The Marker Generation circuitry produces markers at 1, 10, and 50 MHz intervals for RF frequencies up to 2.4 GHz (below 1 Ghz for 1 MHz markers).

A coupler samples the RF from the frequency RF path. This is combined with the frequency comb of a crystal oscillator to produce "marker birdies" when the RF frequency is an integer multiple of the crystal oscillator frequency. The birdies are then discriminated to produce centered marker pulses of uniform width. These pulses can be routed to the ALC loop to produce amplitude markers, or sent to the 8350A Sweep Oscillator to provide Z-axis intensity markers.

RF Section

The RF Section includes the high-frequency microcircuits and their bias components which produce, amplify, and control the amplitude of the RF output.

The 0.01 to 2.4 GHz frequency range is covered with a YIG Oscillator (YO) as the tunable source. A fixed 3.8 GHz oscillator is used to mix down the YO output, thus covering the 0.01 to 2.4 GHz range.

A directional coupler with a detector senses the RF power level and sends a voltage to the ALC circuits for internal power leveling. Another coupler samples the output for use in the Marker Generation circuits.

In Option 002 instruments, a programmable step attentuator is included to provide up to −70 dB of additional output power control range.

DETAILED BLOCK DIAGRAM DESCRIPTION

DIGITAL CONTROL/FRONT PANEL

A3 Digital Interface

The A3 Digital Interface Assembly acts as the 83522's distribution center, receiving digital commands from the 8350A Sweep Oscillator and routing them to the appropriate assembly within the plug-in.

The Buffer receives the digital control (including timing), data, and address signals from the 8350A Sweep Oscillator's Instrument Bus. The control and address lines are uni-directional and pass only to the plug-in, whereas the data lines are bi-directional and carry information both to and from the plug-in. A single buffer returns the plug-in flag (L PIFLG) to the 8350A, indicating that a plug-in front-panel key was pushed.

The Address Decoder provides the major control lines which eventually direct data to the correct part of the plug-in. Address and control lines are decoded to produce "enable lines": two for ROM; three for the Configuration Switches/ Interrupt Control; five for the Front Panel; and two for the remainder of the plug-in assemblies.

The ROM (Read Only Memory) stores program software and constants used by the 8350A microprocessor while executing routines dedicated to the plug-in. Two address decoding lines plus twelve address lines select the byte of data to be sent back to the 8350A.

The Configuration Switch/Interrupt Control circuits serve a dual purpose. The Configuration Switch encodes information about the plug-in (including frequency range, power, etc.), options used, and certain user-defined parameters. During INSTR PRESET and power-on, the switch positions are read by the 8350A microprocessor, then used to display the correct frequencies, markers, power, and other parameters which vary from plug-in to plug-in. As Interrupt Control, the circuits monitor the L SIRQ line, and send an interrupt (L PIIRQ) to the 8350A to begin the bandswitch in multi-band plug-ins. During bandswitch, the Interrupt Control is programmed to count down time intervals specified by the microprocessor. At the end of these intervals, the L PIIRQ line is again activated to notify the 8350A that the time interval has elapsed.

The RF Plug-in Interface buffers the data and address lines for use throughout the rest of the RF plug-in. The data bus is bi-directional, so that the 8350A can read information from the A2 Front Panel Interface and A6 YO Driver assemblies. The control lines, which complete the internal bus, come directly from the Address Decoder. This internal bus sends controls messages and data for DACs to Digital Interface circuits on each assembly. These digital interface circuits are essentially buffers between the digital and analog circuits.

A2 Front Panel Interface
A1 Front Panel

NOTE

Due to their strong functional interrelation, the A2 Front Panel Interface and A1 Front Panel assemblies are discussed together.

The A2 Front Panel Interface and A1 Front Panel assemblies are primarily responsible for displaying the status and power level of the RF plug-in, and transmitting pushbutton and RPG commands back to the 8350A Sweep Oscillator for processing. Front panel analog adjustments, and the analog 1V/GHz rear-panel output, are also processed on these assemblies.

The Keyboard/Display Interface performs two functions. As a Keyboard Interface, it strobes the columns of the Pushbutton Switch Matrix, while sensing the row lines. When a key is pushed, the row line tracks the strobed column line corresponding to that key. The Keyboard Interface detects this, sets the FLAG line to alert the microprocessor, and transmits the encoded key information back to the 8350A for processing. As a Display Interface, the same column strobes are buffered and used to drive the digits of the Power Display. While a digit is enabled, the appropriate seven-segment data, stored inside the Display Interface, is buffered to drive the segments. The scanning is done at a fast rate to avoid flickering.

The Annunciator Interface stores data to drive the LED Annunciators which display the status of various functions. Two special annunciators – MARKER and UNLEVELED – are not digitally controlled, but are driven from separate Mkr/Unlvl circuits which monitor the Marker and ALC assemblies.

The Power Control Interface digitally controls several functional areas. Three of the lines are buffered by the Attenuator Control, which operators the A19 Step Attenuator in instruments equipped with Opt 002. The RF On circuits control the biasing for the A12 YIG Oscillator and A14 Amplifier. When the RF is turned off, the bias to these assemblies is removed, shutting off the oscillator and amplifier.

The Frequency Tracking Amplifier and 1V/GHz blocks are the only active analog circuits on the A2 and A1 assemblies. The Frequency Tracking Amplifier monitors the YO DRIVE V, a voltage proportional to the YO's frequency. Its output tracks the RF output frequency, and is used to compensate for frequency-dependent nonlinearities in the ALC loop. The 1V/GHz circuit further processes this signal to produce a rear panel output supplying 1Vdc per GHz of output frequency for use with external equipment.

Miscellaneous front panel controls must pass through the A1 and A2 assemblies. The RPG produces pulses when rotated, and sends them directly back to the 8350A Sweep Oscillator to be decoded and processed to adjust the power. The FREQ CAL adjustment is used to fine-tune the RF output frequency to correct for drift or error in the frequency of the A16 Cavity Oscillator. The EXT/MTR ALC CAL adjusts the absolute power level when external detector or power meter leveling is used.

FREQUENCY CONTROL

The Frequency Control section of the plug-in is responsible for determining the actual RF output frequency. Based on the tuning voltage VTUNE and digital data, the correct current is developed to tune the A12 YIG Oscillator. Frequency modulation is also processed in these circuits.

A6 YO Driver
A9 Reference Resistor Assembly

The A6 YO Driver and A9 Reference Resistor assemblies scale and offset the tuning voltage from the 8350A Sweep Oscillator, converting it into a current for controlling the A12 YIG Oscillator frequency.

The tuning voltage, VTUNE, is buffered and inverted before being scaled, offset and summed with various correction signals to produce the tuning current for the A12 YIG Oscillator. The full 0 to 10V VTUNE must tune the oscillator from 3.81 to 6.2 GHz.

The Scaling and Offset DACs are also used to compensate for small differences in oscillator sensitivities. The amount of scaling and offset can be set by the Frequency Cal switches. At power-on or Instrument Preset, the status of the Cal switches is read by the 8350A and stored in RAM. This information is then used to program the DACs. The −10V Ref generates a stable voltage source used as a reference on both the A6 YO Driver and A4 ALC assemblies.

The +20V Tracking circuit monitors the +20V supply, producing an output which follows this voltage. The current through the YO is referenced to this supply, this prevents power supply drift or noise from creating frequency errors.

The summing junction adds together the scaled tuning voltage, offset, +20V tracking voltage, and offset compensation, plus the front-panel FREQ CAL. The Delay Compensation from the A7 Marker assembly and LO FREQ FM from the A5 FM Driver assembly (both described below) are also added. The result is the YO DRIVE V, a signal proportional to the YO frequency.

The remainder of the A6 circuits and the A9 components convert the YO DRIVE V to a current to control the YO frequency. The final current drive transistor (A9Q1) is controlled by the A6 assembly. The current through this transistor, and hence the YO, generates a proportional voltage across the Reference Resistor, which is monitored and compared to the YO DRIVE V. Any errors between the two are corrected in a closed loop, producing a current proportional to the YO DRIVE V. Compensation elements (Comp) correct for nonlinearities in the YO. If the YO is replaced, this section of circuitry may also require changing.

In CW mode, a relay connects a large capacitor across the YO's coil. The capacitor resists changes in the YO current to reduce residual FM noise.

The Freq Cal Switches/Status block has two functions. During **INSTR PRESET**, the Freq Cal Switches, set when the plug-in is calibrated, are read for use in setting the Scale and Offset DACs. This information sets frequency end-point accuracy. This section also reads the sweep status and unleveled condition for use by the microprocessor.

A7 Marker

The Delay Compensation circuit on the A7 Marker assembly produces a signal to compensate for time delay in the YIG Oscillator response. The coils in the YO are used to set up a strong, controlled magnetic field to control the RF frequency. Due to inductive and magnetic delays of the electromagnets, there is a delay between the applied voltage and resultant current flow through the coils. The Delay Compensation circuitry monitors the scaled tuning voltage, and from its amplitude and slope produces a signal added to the YO DRIVE V to compensate for swept frequency errors that would occur because of the response delays.

The Oscillator Bias section produces the bias voltage needed by the A12 YIG Oscillator. The YO's correct bias point is dependent on its frequency, so the YO DRIVE V is used to make these frequency-dependent adjustments. The L RFON line will turn off the bias and shut down oscillations altogether when the RF is turned off.

A5 FM Driver

The A5 FM Driver assembly splits the external FM signal, passed through the mainframe, into two paths. One is added to the main coil tuning voltage; the other is routed to a separate coil inside the YO, dedicated to high-frequency FM.

One FM path is lowpass filtered, removing high-frequency components; the other is highpass filtered, removing low-frequency components. The filters are matched in stop-band response, such that one picks up where the other leaves off. Both paths are amplified, and sent through Sensitivity Select circuits which determine the FM sensitivity (i.e. MHz of deviation per volt) and select either cross-over or direct coupling. The LO FREQ FM is eventually added to the YO DRIVE V, and modulates the output frequency through the YO's main coils. However, the main coil cannot respond to fast deviations due to inductive and magnetic delays. Hence, a completely separate, small, but fast-acting FM coil is built into the YIG Oscillator. The HI FREQ FM is sent to this coil, allowing limited high-frequency FM.

ALC / POWER CONTROL

The A4 ALC assembly, and parts of the A5 FM Driver assembly, are responsible for power level control. Power leveling is accomplished by detecting the output RF power level, comparing it to a fixed reference voltage, and adjusting the RF modulator to correct for power errors. This results in constant RF power level across the entire sweep. The absolute RF power is digitally controlled, and can be set between +13 and −2 dBm. (Instruments with Option 002 use an RF Step Attenuator to achieve power control down to −72 dBm. However, this is not part of the leveling loop.) The power sweep and power slope functions are obtained by adding a scaled voltage ramp offset to the reference power level.

A4 ALC Assembly

The A4 ALC assembly receives its inputs from one of the two detectors, and selects one of them for leveling. The sources include DC1 Directional Dectector, the "External" input (external negative detector), and a third position which inverts the polarity of the external input (power meter detection). The selected detector voltage is proportional to the peak RF amplitude. The Input Sample & Hold stores the detected level during pulse modulation. This prevents subsequent circuits from saturating when the RF power drops out during blanking or pulse modulation. The Logger amplifier produces a voltage proportional to the log of peak RF amplitude, and essentially represents the RF power level in dB.

The reference, or desired, power level is established digitally by a 12-bit DAC, scaling the −10V REF from the A6 assembly. This establishes a voltage proportional to the desired output level in dBm. The External AM signal from the 8350A Sweep Oscillator, and the PWR/SWP COMP signal from the A5 FM Driver assembly (described below), are summed in to produce PWR REF.

The second summing junction adds two more component signals. One is the External Cal, an offset voltage from the front panel used to calibrate absolute power when external leveling is used. The 1 dB Marker signal from the A7 assembly is also added, producing a dip in the RF output power when amplitude markers are activated. The final product of the power reference chain is a reference voltage representing the desired RF output amplitude.

The ultimate goal of the leveling loop is to make the actual RF power equal to the desired RF power. A third summing junction compares the voltages representing these two quantities, and yields a signal representing the error between actual and desired power. An additional error voltage is injected at this point to compensate band flatness only. This error voltage is sampled and held during pulse modulation to prevent subsequent circuits from saturating. The held error signal is amplified, and the RF blanking signal added to modulate the RF power for pulse modulation, without saturating any other components in the path. The Modulator driver then provides the current drive needed to control the diode modulator in the RF path. A pulse input to the MOD driver provides pulse modulation. An additional circuit monitors the input to the modulator drivers, and lights a front panel UNLEVELED LED if this voltage exceeds the normal range for leveled power.

A5 FM Driver

The A5 FM Driver assembly includes circuits to produce the PWR/SWP COMP signal added to yield the PWR REF. The Power Sweep function is achieved by scaling the VSW sweep voltage with a DAC. By programming the appropriate scale factor, a voltage representing dB/GHZ or dB/Sweep is produced.

The ALC Compensation is a four-breakpoint, adjustable slope network which compensates for fixed frequency-dependent nonlinearities in the RF path, typically the coupler. Its input is FREQ TRK V, a voltage exactly proportional to frequency. This signal drives an array of four transistors, and their outputs are summed together to yield the ALC compensation signal. The gain of each transistor, and the voltage at which that transistor begins to conduct, are adjustable. A ninth adjustment adds the FREQ TRK V directly. In this way, a complicated compensation function, approximated by five straight lines, is produced.

The Power Sweep DAC adds a ramp voltage to the power reference signal when the Power Sweep or Power Slope functions are activated. Its input, VSW, is a sweep ramp that essentially tracks the tuning voltage but always runs from 0 to 10 Vdc. A digitally programmable multiplying DAC scales this voltage according to the dB/SWP or dB/GHz value selected. (If these functions are disabled, the DAC is set to its minimum value.) This ramp is added to the ALC Compensation signal described above, and added to the Power Ref signal on the A4 assembly.

MARKER GENERATION

The 83522A features both amplitude and intensity markers at multiples of 1 MHz up to 1.0 GHz, and multiples of 10 or 50 MHz up to 2.0 GHz. They are derived from a crystal, and hence are extremely accurate and stable.

A8 Sampler Assembly

A crystal-stabilized 50 MHz oscillator on the A8 Sampler assembly provides the reference frequency for the markers. This squarewave is divided by five, then divided by ten again, making squarewaves at 50 MHz, 10 MHz, and 1 MHz available. A switch selects one of these outputs to be used, depending on the front panel function selected. The squarewave passes through a comb generator, making a pulse train containing many harmonics at integer multiples of the input frequency. This is then mixed with the RF output sampled by the DCI Directional Detector, producing many mixing products at the sum and difference frequencies of the RF frequency and each harmonic of the comb generator.

The external marker is produced by mixing the RF output with an externally-produced signal (EXT MKR) below 2.4 GHz in a second mixer. The sum and difference frequencies are then processed just as the harmonic sum and difference frequencies.

The mixing products are passed through a lowpass filter with a programmable cutoff frequency. This filters off the high-frequency mixing products and allows only the low-frequency product to pass. When the RF output frequency is being swept, the resulting string of "birdies" reach peak amplitude when the mixing product frequency approaches zero.

The "birdies" are buffered by an amplifier with a controllable gain. A Gain Shaping circuit monitors the reference power level and adjusts the gain to compensate for varying levels of SAMPLED RF. This maintains uniform "birdie" amplitude as power level changes.

The "birdies" pass through a switch opened by the LPULSE line, disabling the marker circuits when the RF power is pulsed. This prevents the power dropouts from producing false markers. A second switch, actuated by the buffered "birdies," transforms the analog signals into a TTL rectangular wave for processing on the A7 Marker assembly.

A7 Marker Assembly

The A7 Marker assembly receives the TTL "birdies" and processes them to generate marker pulses that are centered where the RF output frequency is exactly equal to a harmonic of the crystal oscillator, producing a mixing "null." A digital circuit detects the time between "birdie" pulses and discriminates this null to produce a marker pulse. This marker pulse produces 1dB markers through the ALC circuits, and sends a pulse to the mainframe to produce Z-axis intensity markers when enabled.

The Pulse circuits are part of the A7 Marker assembly. The Pulse circuits essentially combine three different pulse sources: Square Mod and RF Markers from the 8350A, and Pulse Input from the plug-in rear panel. The output (L PULSE) shuts off the RF, acting on the A17 Modulator/Mixer through the A4 ALC assembly.

RF SECTION

The RF Section includes the microcircuits and their bias boards that produce the actual RF output power. These components include A11 through A19 and DC1.

The A12 YIG (Yttrium-Iron-Garnet) Oscillator (YO) is the frequency-controllable microwave source for the 83522A RF Plug-in. The YO's frequency is determined by the current flowing through large electromagnetic coils inside. This current is the result of summing and scaling operations performed by the A6 YO Driver and A9 Reference Resistor assemblies. Due to the response-time limitations of the main coils, a smaller coil with a much faster response, but limited range, is used to modulate the output frequency.

The YO's 3.81 to 6.2 GHz output is fed to the A17 Modulator/Mixer. Here it is mixed with the fixed 3.8 GHz output of the A16 Cavity Oscillator, yielding the heterodyned output from 0.01 to 2.4 GHz. Power control and leveling is accomplished by modulating the 3.8 GHz input before the mixer, internal to the A17 Modulator/Mixer.

A14 Amplifier boosts the mixed-down low-power output from the A17 assembly. The amplifier also serves to further remove unwanted high-frequency mixing products. The A14A1 Amplifier Bias assembly is directly connected to the microcircuit, has no adjustable or replaceable parts, and is not separately replaceable.

The A15 DC Return allows DC currents to pass to ground, preventing them from affecting other circuits.

DC1 Directional Detector serves a dual purpose. A broadband resistive bridge couples off a portion of the RF energy, rectifies and filters it, and provides a detected output for leveling. Another resistive tap samples the RF power for the Marker Generation circuits.

The RF output is finally directed to the front panel RF Output connector. On instruments with Option 004, different RF cabling takes the output to the rear panel connector. On instruments with Option 002, the A19 RF Step Attenuator is included, providing from 0 to 70 dB of attenuation in 10 dB steps. This attenuated output is then routed to the front panel connector (Option 002 only) or rear panel connector (Option 002 with Option 004).

83522A OVERALL TROUBLESHOOTING

The purpose of this troubleshooting information is to provide an aid in isolating a problem in the 83522A to a specific assembly. Further troubleshooting information is supplied with each service sheet to isolate the problem to the component level.

The first step in overall troubleshooting is to identify the symptom(s) and determine under what conditions the problem exists. If the problem is an RF plug-in error code (E001 or E050 through E053) refer to the Error Code section of this troubleshooting procedure. Also ensure that the 8350A used with the 83522A is calibrated and functionally operating.

A failure in the 83522A normally affects one of the following functions.

- Front Panel/Digital Control – Probable symptoms are error code E001, incorrect annunciator or digit displays, inability to control operation from front panel, or erratic instrument response to front panel entries. The problem is generally on the A1, A2, or A3 assemblies, or with the RF Plug-in/8350A interface.

- Frequency Control – Frequency control problems include frequency inaccuracy and sweep control problems. If the 8350A VTUNE output and power supplies are verified, the problem is most likely on the A5, A6, or A9 assemblies, or in the RF Section. If a frequency accuracy problem occurs only during swept operation, and the inaccuracy increases with faster sweep times, the problem is most likely with the Delay Compensation circuit on the A7 Marker assembly.

- Power Control – Typical problems are no RF Output, maximum unleveled RF output, or excessive power level variations. The problem is most likely with the A4, A5, or RF Section. If the trouble is limited to power sweep and slope control, the problem is most likely with the Power Sweep DAC on the A5 assembly.

- Marker Generation – Typical problems are that markers are generally unstable or not present. Problem may be frequency related. Typically, the trouble is with the A7 or A8 assemblies, or the RF Section. If problem is with amplitude markers only, trouble may be with the A4 ALC assembly.

- RF Path – Problems associated with high-frequency microcircuits include spurious or harmonic distortion, no RF power, or full unleveled RF power. For a harmonic distortion problem, refer to Section V, Adjustments. For power problems, refer first to the A4 ALC Troubleshooting before suspecting the RF components.

Once the problem is identified, exercise the RF plug-in to determine under what conditions the problem exists. Some important conditions to check are:

- Sweep Mode related – Is problem only for swept modes of operation, or does it also exist in CW operation? If problem still exists in CW operation, troubleshoot in this mode (it is easier to check waveforms and voltages in CW operation).

- Control related — Try different methods of entering data (i.e. RPG, Data Entry Keys, or increment/decrement keys). If the problem is related to a specific control, troubleshoot that control and respective circuits. If the problem is related to a specific type of control (i.e. pushbuttons) refer to the A1/A2 service sheet and troubleshoot the respective interface circuit.

- Sweep Time related — Swept frequency accuracy problems that get worse with faster sweep times are probably caused by the Delay Compensation circuit on the A7 assembly.

Error Codes

RF Plug-in error codes are displayed in the 8350A left FREQUENCY display. The error codes may be generated as a result of the Instrument Preset self test (E001, E052, or E053), or during normal instrument operation (error codes E050 or E051). A description of each error code is provided in Table 8-5. Further troubleshooting information for each error code follows.

Error Code E001. Error code E001 indicates that the 8350A microprocessor is unable to properly read plug-in ROM. Initial checks should be made to verify proper mating of rear panel connectors with the 8350A. Also check cable connections to the A3 Digital Interface and ensure A3 is properly installed. Refer to the A3 service sheet for specific troubleshooting information.

Error Code E050. Error code E050 is generated when the 8350A microprocessor responds to an RF Plug-in keyboard flag (L PIFLG) and no key has been pressed. Check the logic state of the FLAG input to the A3 Digital Interface (A3P1 pin 42). It should be a stable logic low until a front panel key is pressed (when it is briefly strobed high). If it is not a stable low, refer to the A2 service sheet for further troubleshooting. If FLAG is a stable low, check that the L PIFLG output of A3 (A3J1 pin 39) is a stable high and pulses low when a front panel key is pressed. If necessary, trace the logic state of PIFLG on the 8350A A3 Microprocessor.

Error Code E051. Error code E051 indicates that an invalid keycode is received by the 8350A microprocessor. Refer to the A1/A2 service sheet to troubleshoot the keyboard matrix and Keyboard/Display Interface circuit.

Error Code E052. Error code E052 is generated if there is a problem with the Interval Timer on the A3 Digital Interface. A test routine is run at power-on or when Instrument Preset self test is initiated. If Error code E052 is generated, refer to the A3 Digital Interface service sheet for further troubleshooting.

Error Code E053. Error Code E053 is generated at power-on or Instrument Preset when there is a problem with the Peripheral Interface Adapter (PIA) on the A3 Digital Interface. If error code E053 is generated, refer to the A3 Digital Interface service sheet for further troubleshooting.

Digital Control/Front Panel

A digital control problem usually affects the entire plug-in, but may disable only a section of the instrument. Generally, a digital control problem is indicated by a front panel failure. If the problem is limited to a specific type of control (pushbutton or RPG) or display (annunciator or digital display), the indication is that of a front panel failure. An RPG failure may indicate problems on the

front panel assemblies of the 8350A mainframe, where RPG pulses are decoded. If multiple front panel functions are inoperative or erratic, the problem is most likely a digital control problem. Detailed troubleshooting procedures for checking front panel operation are provided in the A1/A2 service sheet. For digital control problems, refer to the A3 Digital Interface service sheet, and check the address, data, and control line outputs of the A3 assembly.

When there is a problem with a digital-to-analog interface (i.e. DAC), the symptom is generally a discontinuity in the analog response.

Frequency Control

Troubleshooting a frequency control problem can be greatly simplified by first defining the conditions under which the problem exists. When troubleshooting, the RF Plug-in should be operating in the least complicated mode that exhibits the frequency control problem. For instance, a CW frequency is less complicated than a swept mode.

NOTE

To ensure accurate frequency counter readings, check for adequate RF output power.

Incorrect Frequency Display after Instrument Preset. If the frequency range displayed corresponds to the frequency range of another RF plug-in, verify that Configuration Switch A3S1 is set correctly. Otherwise, there is a digital problem.

Frequency Accuracy Problems. Frequency accuracy problems are most likely related to the front panel FREQ CAL adjustment. Refer to Section III for the FREQ CAL adjustment procedure. The YO DRIVE V on the A6 YO Driver can be checked by comparing the rear panel 1V/GHz output with frequency selected and the actual RF output frequency. Connect a digital voltmeter to the rear panel 1V/GHz output. Compare the digital voltmeter indication with the 8350A FREQUENCY display and the actual RF OUTPUT frequency. If the voltage corresponds to the actual output frequency, perform the Frequency Accuracy adjustment in Section V before further troubleshooting.

Swept Frequency Accuracy Problem. A frequency accuracy problem that occurs only during swept frequency modes is typically a delay compensation problem. Refer to the A7 Marker for further troubleshooting.

Power Control

Power control problems normally fall into one of the following catagories.

- No RF Output Power
- Maximum Unleveled RF Output Power (no power control)
- Excessive power variations

No RF Output Power. Remove the A4 ALC assembly; the RF OUTPUT power should go to a maximum level. If not, the trouble is in the RF Section. If the RF OUTPUT goes to maximum, the problem is in the A4 ALC assembly.

Maximum Unleveled RF Output Power. Check leveling in External and Meter leveling modes. If power is leveled for these modes, the problem is with the internal detector. Otherwise, refer to the troubleshooting information for the A4 ALC assembly.

Excessive Power Variations. Refer to the troubleshooting information for the A4 ALC assembly.

Marker Generation

Marker generation problems are generally associated with the A7 Marker or A8 Sampler assemblies. Performance of the Marker and Sampler adjustments is a good troubleshooting aid for unstable or no marker operation. If the marker problem is related to external markers only, perform the External Marker adjustment. If the marker problem is dependent on whether amplitude or intensity markers are selected, the problem is most likely with the A4 ALC for amplitude, and the 8350A, or interface, for intensity markers.

If external markers are operational and internal markers are not available, check the Sampled RF output from DC1 and the 50 MHz oscillator operation on the A8 Sampler.

RF Section

RF Section problems are usually indicated by no RF Power, full unleveled RF power, excessive harmonics, or spurious responses. For an RF power problem refer to the Power Control section of this troubleshooting information. For excessive harmonics or spurious responses, refer to the RF Section service sheet for further troubleshooting.

Table 8-5. 83522A Error Codes

Error Code	Function Tested	Operator Initiated Test	Troubleshooting Hints
E001	8350A/83522A		Check the RF plug-in connections and cable connections to A3. Do Hex Data Write to front panel and Hex Data Read of A3S1 Configuration switch. See E001 Troubleshooting in this procedure for specifics.
E050	Plug-in keyboard		Check PIFLG
E051	Invalid key code	SHIFT 04	See A1/A2 service sheets for further troubleshooting.
E052	Interval Timer	SHIFT 55	See A3 service sheet for further troubleshooting.
E053	PIA	SHIFT 55	See A3 service sheet for further troubleshooting.

annunciators are buffered by inverters, and drive current through the LED to ground rather than sinking current from +5V. The outputs of these buffers can be checked during Hex Data Rotation Write.

MKR and UNLEVELED lights are driven by pulse-stretching timers. These are disabled by U9A during retrace. Check that U9, pin 3, is high during retrace (approximately +4Vdc), and low during forward sweep. The UNLEVELED light should be lit when the available power is insufficient for leveling to the desired reference level (typically several dB beyond specified maximum leveled power).

If the L MKR light is not functioning properly, set the 8350A as follows: Start sweep = 30 MHz, Stop sweep = 90 MHz, Time = 500 msec. Select 83522A 1 MHz MARKERS. Connect oscilloscope channel B to the 8350A Sweep Out, and select the A vs B mode for horizontal deflection as a function of the 8350A sweep ramp. Check the input (pin 8) and output (pin 9) of timer U12B. The output of U12 goes high for an initial low pulse at the Trigger input (T), and remains high for a period of approximately 50 milliseconds. Subsequent trigger pulses, occurring within the timing cycle, will not affect the output. However, if the Trigger input remains low for a longer duration than the timing cycle, the output will remain high for the duration of the trigger signal. If no trigger signal is present, check diodes CR4 through CR7, or trace the problem back to the A7 assembly.

If the UNLEVELED light is not functioning properly, select 8350A **RF BLANK** and disengage 83522A RF to turn the power off. In this mode, LUNLVL, J1-12, should be low during forward sweep, and high during retrace. Connect oscilloscope Channel B to 8350A Sweep Out and select the A vs. B mode for horizontal deflection as a function of the 8350A sweep ramp. Check the input (pin 6) and the output (pin 5) of timer U12A. Refer to the previous paragraph for an explanation of U12. If the circuit is functioning properly, trace the problem back to the A4 assembly.

Keyboard

The keyboard matrix is scanned continuously by U6. This LSI device continuously strobes the column lines, senses the row lines for depressed keys, eliminates contact bounce, stores the key code internally, and flags the 8350A to recover the key code. Troubleshooting is difficult because the device is so complicated, but it is worthwhile to check all signals to and from U6, probing directly on the pins of the chip, before replacing it.

Error codes E050 and E051 generally indicate U6-related problems:

- E050 occurs when the microprocessor has received a flag (L PIFLG) from the plug-in (indicating a front panel key was pressed), but cannot recover the keycode (indicating that the key was NOT pressed). Check the FLAG output from A2U6 (accessible at A3P1-42). It should be TTL low, approximately 0 volts. Pressing a front panel pushbutton should result in a very rapid pulse. If the line appears to be locked high, replace A2U6. If it is good, check inverter A3U10F (accessible at A3J1-39) to see if it is locked low.

- E051 occurs when the key code received by the microprocessor cannot be decoded. This indicates a failure in A2U6 or a bad Row Sense line. If the Row Sense lines are good, troubleshoot the keyboard matrix with a continuity checker.

To troubleshoot the plug-in keyboard matrix, initiate the Key Code Test. Enter **SHIFT 0 4** . Thereafter, when pressing any plug-in front panel key, the appropriate hexadecimal key code should appear in the mainframe FREQUENCY/TIME display window. The appropriate key codes are given in Table 8-6.

If this test indicates further troubleshooting, remove the front panel to make A2 accessible while connections between the front panel, plug-in, and mainframe are still intact.

If the numerical display is blank, check power supplies on A2.

Check U6, pin 3, for the 200 kHz SCAN CLK signal. If it is missing, trace the problem back through U4B to the A3 Digital Interface assembly.

Initiate Hex Data Rotation Write and check the L FP2 line for activity:

SHIFT 0 0	Hex Data mode
2 MHz ms 8 0	Address location 2d00 (U6)
M4	Hex Data Rotation Write

The data line inputs should also be checked in this mode. The pattern should match that shown in Figure 8-2.

Check the COL0 through COL3 lines for sequential low pulses, as shown in Figure 8-14.

If the patterns are absent, but the 200 kHz clock is present, the problem is probably U6. Ensure that problems in U4B or the A1 assembly are not tieing the lines down.

If the column strobes are present, probe both the column and row line corresponding to the key in question at U6. Observe the traces while pushing the button. The two lines should track each other. If they track, but the microprocessor can't read the codes from U6 and the data bus is good, the problem is probably in U6.

If row and column do not track, separate the A1 and A2 assemblies and troubleshoot the keyboard matrix with a continuity tester.

Rotary Pulse Generator (RPG)

The RPG is a means of converting rotational information into digital signals which can be read by the microprocessor. The hardware components needed to decode the plug-in RPG (counter and sign latch) are located on the 8350A A2 Front Panel Interface assembly. Some failures which appear to be in the plug-in RPG, (e.g., 'run-away' POWER display or a locked-up sign) are likely to be caused by failures in the 8350A.

If the plug-in RPG appears to be dead, remove the bottom cover of the 8350A and probe A10J1, pins 34 and 36. Check for the waveforms shown in Figure 8-15, while slowly rotating the RPG. If the signals are present, trace the PIRPGA and PIRPGB lines through the 8350A to the mainframe A2 assembly. Refer to 8350A A2 Service Sheet for more information.

If the signals are absent in the plug-in, check for the +5V at A10J1, pin 2. Then remove the front panel and check for +5VR directly at the point where the RPG leads are soldered to the A1 Front Panel assembly. Then probe the two RPG output leads for the waveforms in Figure 8-15. If they are absent, check that the output lines are not shorted to ground. If not, replace the RPG.

Analog Circuitry

Analog circuitry on the A2 Front Panel Interface processes the YO DRIVE V signal to produce the 1V/GHz rear panel output and FREQ TRK V, used in the ALC loop.

Check that the YO DRIVE V signal is present at TP1. It should resemble the waveform shown in Figure 8-16. If it doesn't, trace the problem back to the A6 YO Driver assembly.

If it is present, check TP3 for the waveform shown in Figure 8-17. If it is present on the A2 assembly, but FREQ TRK V is missing on the A4 and A5 boards, probe the emitter of Q3 for the same waveform offset by approximately 0.6 Vdc.

Analog switches U9B, U9C, and U9D are controlled by latch U8. These switches apply an offset to FREQ TRK V, and turn it off when external leveling is used. These switches can be exercised by using Hex Data Write. Press 8350A **CW** and enter:

SHIFT 0 0	Hex Data mode
2 **BKSP** 0 0	Address location 2F00 (U8)
M2	Hex Data Write
0 0	Enters hex byte 00
BKSP **BKSP**	Enters hex byte FF

Note that these switches are not identical. U9B is open for logic 0, while U9C and U9D are closed.

The 1V/GHz Amplifier adds one more stage of gain and offset to FREQ TRK V, producing a scaled tuning ramp to follow the RF output frequency at exactly 1 Vdc per GHz. Check the rear panel 1V/GHz BNC output jack for the ramp. If it is absent, check TP2 for the waveform shown in Figure 8-18. If there is no signal at TP2, but there is a ramp at TP3, the problem is in U1A.

RF Power Control Latch

U8 stores commands for the RF Step Attenuator (Option 002 only) and the RF ON line, which supplies −10V bias for components in the RF path. It also controls analog switches used for the signals mentioned above.

Hex Data Rotation Write can be used to verify the outputs of U8.

NOTE

In Option 002 plug-ins, disconnect the attenuator cable at A2J3 before initiating Hex Data Rotation Write. The bit pattern shifts too fast to actuate the attenuator properly, and may damage it.

Initiate the check as follows

SHIFT 0 0	Hex Data mode
2 **BKSP** 0 0	Address location 2F00 (U8)
M4	Hex Data Rotation Write

Check L FP5 line for activity. Check data lines for patterns illustrated in Figure 8-2.

To check the RF ON relay, K1, make the same key entries as above, except enter **M2** for Hex Data Write. Then alternate between data inputs: **0 0** and **BKSP BKSP** (FF). The RF ON line should toggle from 0 Vdc to −10 Vdc. If there is no change, check U8, pin 12, for high and low levels. If the output is locked high, check the protection diode, CR3, before replacing U8. However, if CR3 is open, U8 may be damaged by actuating the relay. If the output at pin 12 is locked low, replace U8. If U8 pin 12 changes levels properly, replace relay K1.

Miscellaneous

The FREQ CAL and EXT/MTR ALC CAL offsets are generated by A1 potentiometers, with the wipers running between +10 Vdc and −10 Vdc. If the signals are absent, check for the +10V and −10V supplies. If the offset voltages still cannot be produced, replace the defective potentiometer, R3 or R4.

First check the 200 kHz Clock. The SCAN CLK line is accessible at U3 pin 3, at the top of the A3 assembly, so it is not necessary to remove the A3 board to test it. The output frequency should be approximately 200 kHz. The pulse train is NOT symmetrical, and has TTL levels. If no clock signal is found, suspect U3.

Error Code E053

If the SCAN CLK is present, yet E052 occurs, then the failure is probably with U5. Press **SHIFT** 5 5 , and check the LWR and LRD lines for the waveforms shown in Figure 8-22. If either control line is inactive, troubleshoot the address decoder U9. If the control lines are working, check the CTR 0 and CTR 1 waveforms as shown in Figure 8-22. If they are incorrect, replace U5.

E053 generally indicates a failure in the PIA, U4. However, the problem might be in the output stages of U5. Enter **SHIFT** 5 5 , and check CTR 0 and CTR 1 waveforms as shown in Figure 8-22. If they are correct, U5 is functional. Next, check the L PIAE line as shown in Figure 8-22, and make sure the L WRITE line shows activity. If not, troubleshoot the appropriate address decoding circuitry or buffer. Then, check L PIIRQ for the squarewave shown in Figure 8-22. If it is inactive, replace U4.

No Error Code

If no error code occurs and the 8350A displays show the correct start and stop frequencies of the plug-in, the Plug-in Self Test passed successfully. This verifies the Instrument Bus to the plug-in, data and address busses on the A3 Digital Inteface assembly, and plug-in ROM. Any plug-in failures which are traced back to the A3 assembly are due to failures in one or more of the following areas:

- Address Decoding
- Plug-in Buffers
- Interrupt Control/Configuration Switch
- Miscellaneous Control Lines

If the 8350 displays show the wrong frequencies, first check configuration switch S1 against Table 8-8, and then troubleshoot the PIA, U4.

Address Decoder

The primary address decoding for the plug-in occurs on the A3 assembly. The enable lines are then passed on to the rest of the instrument. The Major Address Decoder Test can be utilized to check all these lines. Enter:

SHIFT 5 3

Then check the outputs of U6B, U6C, U7B, U9, and U13 for the signals shown in Figure 8-23. The address lines have been verified by the Self Test. Therefore, if the LPIAE or ROM enable lines are faulty, troubleshoot the discrete address decoding logic involving U6, U7, U8, and U10, and replace the defective component. If other pulses are missing or displaced, replace the appropriate decoder, U9 or U13.

Plug-In Interface

U14 and U17 buffer the address and data lines for use throughout the plug-in. The address and data busses on the A3 assembly have been verified by the Instrument Preset Self Test. Therefore, if address or data is not being passed to another assembly, the fault lies with U14, U17, U6A, or a motherboard connection.

The address lines can be exercised by performing the Minor Address Decoder Test. On the 8350A, enter:

SHIFT 5 4	Minor Address Decoder Test

Verify activity on each of the buffered address lines (BA0 – BA3).

Data lines can be verified by performing a Data Rotation Write to any address location between 2C00H and 2FFFH. On the 8350A, enter:

CW	Set 8350A into CW mode
SHIFT 0 0	Enters the Hex Data command
2 **GHz s** 0 0	Address location 2C00
M4	Hex Data Rotation Write

Check for activity on each of the buffered data lines (BD0 – BD7), and check for shorts between lines.

Interrupt Timer/PIA

The PIA is responsible for two functions:

- Reading the Configuration Switch
- Routing the L SIRQ Interrupt from the A6 Assembly

NOTE

Before changing the Configuration Switch settings, note the switch positions and return the switches to their original settings after troubleshooting.

The PIA's read capability can be checked by entering:

CW	Sets the 8350A into CW mode
SHIFT 0 0	Enters Hex Data command
2 9 0 0	Address location 2900
M3	Hex Data Read

Watch the display change as the Configuration Switch is toggled.

The Triple Timer and PIA's interrupt masking capability are tested using a special routine at INSTR PRESET or power-on. Error Codes E052 or E053 are displayed if a failure is detected. If these error codes are found, or if either U4 or U5 are suspect for other reasons, a special test pattern can be accessed by entering:

SHIFT 5 5	Interrupt Control Test

The waveforms shown in Figure 8-22 should be observed. Refer to "Other Error Codes" for details on these errors codes and the **SHIFT** 5 5 Operator Initiated Self Test.

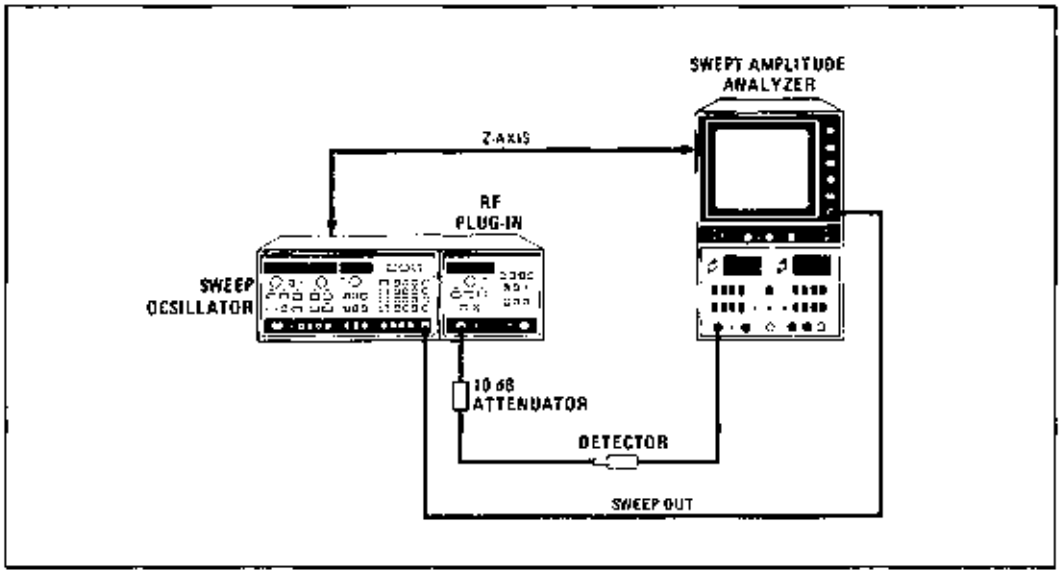


Figure 8-26. Typical ALC Troubleshooting Setup

RPG/Power Display Failure

Check that the POWER display changes when either the RPG is rotated or data is entered via the 8350A keyboard. This verifies that the digital information is reaching the mainframe, is properly processed, and then displayed.

- If the display is flashing rapidly or showing random patterns, refer to A1/A2 Front Panel or A3 Digital Interface troubleshooting. If the RPG causes a change in the measured RF power level, but the POWER display remains the same, refer to A1/A2 troubleshooting. If the RPG produces no response whatsoever, or if the front panel display is blank, refer to A1/A2 troubleshooting, and trace the problem back to the 8350A mainframe.

Unleveled (LED)

If the UNLEVELED light turns on during the sweep, enter a sweep time of 2.4 seconds (i.e. one second per GHz). Observe the SWP light on the 8350A Sweep Oscillator, and determine at which times during the sweep the UNLEVELED light turns on.

- If the UNLEVELED light remains lit during retrace, suspect problems in the front panel annunciator drivers. Refer to A1/A2 troubleshooting.

- If the UNLEVELED light blinks briefly at the beginning of the sweep, the plug-in may be sweeping through 0 Hz and causing an ALC drop-out. Check this by slowly increasing the start frequency. If the UNLEVELED light stops blinking, enter a CW frequency of 50 MHz and enable the 50 MHz crystal marker. Slowly adjust the 83522A front panel FREQ CAL knob until the MKR light stays on. Press **INSTR PRESET** and observe the UNLEVELED light. A frequency counter may be used to check frequency accuracy at 10 MHz or 50 MHz. If necessary, refer to Section V, Adjustments, in this manual, and perform the Frequency Accuracy calibration procedure.

- If the UNLEVELED light flashes briefly during the sweep, but does not imply any of the above failure modes, check power flatness. See below.

Flatness/Oscillations (Power Drop-outs)

Monitor the RF output with the HP 8755C as shown in Fig. 8-26.

- If the power level is constant across the sweep within approximately 5 dB, then the plug-in may only require ALC flatness adjustments. Refer to Section V, Adjustments, in this manual, for the Internal Leveled Flatness adjustment procedure.

- If the measured power level lies between +13 and −2 dBm, but can't be controlled via the front panel, refer to the Digital Control section under Troubleshooting Diagnosis.

- If the trace appears chopped or broken the loop may be oscillating. Refer to Section V. Adjustments, in this manual, and perform the ALC Gain adjustment procedure.

Full Unleveled Power

Set the 83522A to sweep the full range.

- Attempt to level the power externally using the HP 432A Power Meter as shown in Figure 8-27. Select **MTR** leveling, and enter a slow (at least 30 seconds) sweep time. If the RF power is now leveled then the failure is most likely in the detector or the Detector Selection Switch, A4U6. Refer to the following paragraph. If this does not prove to be the case, the problem may be in the two analog switches U4B and U6A. It may be necessary to perform the ALC adjustments in Section V of this manual.

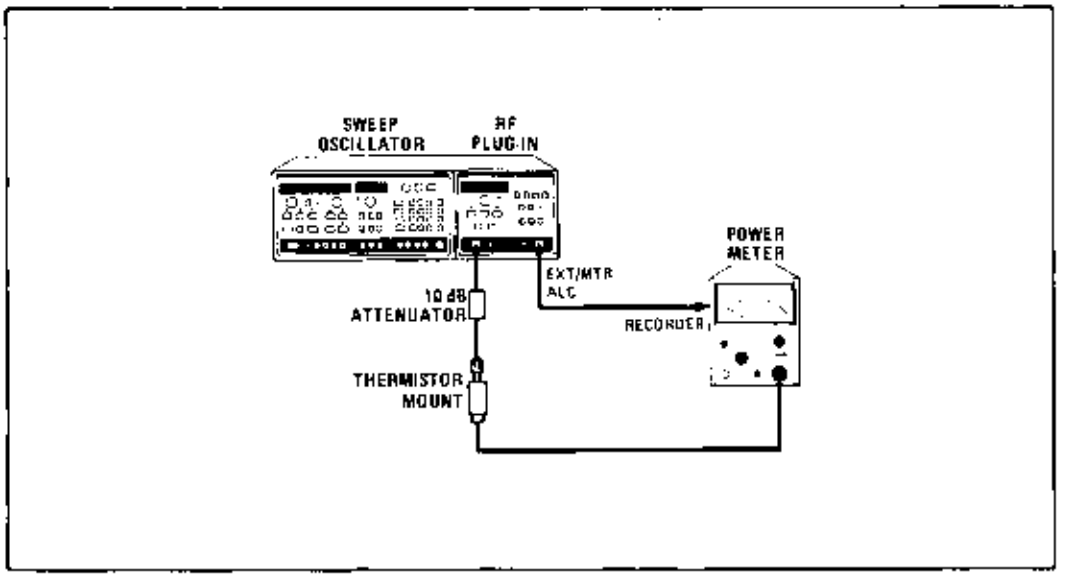


Figure 8-27. Power Meter Leveling Setup

- Check the Detector Selection Switch by entering a CW frequency at the desired frequency or in the leveling mode in question and trace the detector voltage through U6B. If the input to be selected doesn't match the output, check the MUXA0 and MUXA1 lines (see Table 8-10). Also check U12 and U13 as described under Digital Control.

- Check the voltage at TP6. If it is at 7.5 Vdc, suspect the PIN Mod 0 Driver or the Modulator. If it is below +4 Vdc, suspect the Detectors and Detector Leg.

No Power

NOTE

Turn off line switch before removing or installing any assembly.

NOTE

With the ALC assembly removed from the plug-in, 27.8 kHz square wave modulation is not available in the 83522A.

- To check the RF components, remove the A4 ALC assembly from its socket. This removes all bias from the modulator and should allow maximum power through the RF path. If full power (over +15 dBm) is then detected, the RF amplifier (A14), cavity oscillator (A16), and DC Return (A15), are verified. Suspect primarily the detector. Also inspect the modulator, as well as the A4 PIN Mod 0 Driver and Detector Selection Switch.

- If power is still missing, enable the plug-in markers and check that the MKR light flashes. If it does, then the failure must be limited to the DC1 Directional Detector. If the markers do not work, check the A12 YIG Oscillator, A17 Mod/Mix, A16 Cavity Oscillator, and A14 Amplifier. Refer to RF troubleshooting procedures for details.

- If removing the A4 assembly causes full unleveled RF power to appear, reinstall the board and check A4TP6. If less than +4 Vdc is found, check continuity from A4TP6 to the PIN Mod 0 Driver circuit. If A4TP6 is at +7.5 Vdc, suspect any circuitry between the Detector Selection Switch and A4TP6, particularly the Log Amp.

Power Sweep/Flatness

- If power increases smoothly with frequency, and POWER SWEEP is NOT selected, suspect problems with the A5 FM Driver assembly.

NOTE

Turn off line power before removing or installing any assembly.

Remove the A5 board from the plug-in. If the situation improves, suspect a failure on the A5 assembly.

- If the RF power is leveled within approximately 5 dB, refer to Section V, Adjustments, in this manual, and perform the Internal Leveled Flatness adjustment procedure.

Troubleshooting Diagnostics

The troubleshooting information below is organized into functional areas:

Digital Control (A)
Reference Power Level (C) (F)
Detector/Detector Selection Switch (B) DCI
Detector Leg (D) (E)
Modulator Leg (G) (I)
Mod Driver (K)
Modulator/Mixer A17

Digital Control (A)

Address Decoder U12 and Control Latch U13 control digital switches throughout the A4 assembly. Their operation can be confirmed by performing the Hex Data Rotation Write at address 2C07 (Hexadecimal). Enter the following key strokes:

SHIFT 0 0	Enters Hex Data Command
2 GHz s 0 7	Address location 2C07 (U13)
M4	Hex data Rotation Write

Check the outputs of U13 for the waveforms shown in Figure 8-2.

- If any output signal is missing or misplaced, check the data lines against Figure 8-2. If no output is found, look for activity at U13 pin 11. Check for L INST1 and BA3 to pulse low, while BA0, BA1, and BA2 pulse high. If these pulses are missing, trace the problem back to A3 Digital Interface.

If the Digital Control section is working, the primary outputs of U13 are easily controlled by selecting the appropriate front panel function while in the CW sweep mode (e.g., selecting MTR leveling holds the PM line high, etc.).

Reference Power Level (C) (F)

The Reference Power Level Leg produces a voltage proportional to the "desired" power level. This signal is a summation of the absolute power reference, AM, amplitude markers, ALC compensation, and power sweep signals.

The ALC compensation and power sweep signals are generated on the A5 FM Driver assembly. If an A5 failure is suspected, refer to troubleshooting information on the A5 Service Sheet. Unless A5 is suspect, simplify A4 troubleshooting by turning off the line power and removing the A5 assembly. Although power sweep will be disabled and the power flatness will be lost, the ALC loop should still level without the signals provided by the A5 assembly.

DAC U14 establishes the absolute power level. The −10V REF from the A6 assembly is scaled to yield from 0 Vdc (−2 dBm displayed) to +10 Vdc (+22 dBm displayed) at TP2. (This breaks down to a voltage step of 0.42 Vdc per 1.0 dB of power over the dynamic range, or 6.25 Vdc at +13 dBm.)

A self-test routine is available to exercise the ALC DAC. Enter:

SHIFT 5 0

The waveform in Figure 8-32 should be seen at TP2. Note that the exercise routine for the 12-bit DAC yields a staircased waveform with 13 levels. The first step shows the maximum +10 Vdc output with all bits high. The following levels represent the voltage at TP2 with successive bits loaded high in order from the Most Significant bit to the Least Significant Bit.

- If the waveform at TP2 is not correct, check for −10V REF, and trace any problem back to the A6 assembly. Look for activity on L INST 1, BA0, and BA1. BA2 and BA3 should pulse high as each new DAC value is loaded, pulsing the CS line (U14 pin 8) low. If any of these lines, or a data line, appears dead, trace the problem back to the A3 assembly.

U3A adds PWR SWP/COMP and AM, and provides detector flatness compensation at higher power levels with CR2. Use the **EXT MTR** mode to bypass these diodes while troubleshooting.

U3C adds the amplitude markers (L 1DB MKR) and the front panel amplitude adjustment (EXT CAL) used with external leveling. The following levels should be seen at TP1 with A5 removed and **INT** leveling selected: +0.3 Vdc for −2 dBm, and +7.0 Vdc for +22 dBm. Amplitude markers produce a 250 mVdc dip when the MKR light is on. An amplitude modulation (AM) signal of 1.0 Vp-p at P1-4 will produce roughly 260 mV p-p at TP1.

Detector/Detector Selection Switch (B) DC1

The DC1 detector is tested simply by checking its output voltages under full leveled power or full unleveled power conditions. The A4 assembly must be installed for troubleshooting as it supplies bias current to the detector.

NOTE

The 27.8 kHz modulation signal required for 8755 compatibility is not available when the A4 assembly is removed from the plug-in.

- If no power is measured, turn off the line power and remove the A4 assembly. Return power to the instrument. (If there is still no RF power, suspect components of the RF path. Refer to RF Troubleshooting.) If full unleveled RF power is obtained, apply a narrow strip of cellophane tape to the pin-edge connector to isolate the output of the PIN Mod 0 Driver from the modulator (P1-44). Reinstall the A4 board. This removes bias from the modulator, allowing full RF power transmission, while providing detector bias.

If full leveled power (+13 dBm) or full unleveled power (at least +15 dBm) is measured, sweep the full band and check the voltages at the detector inputs against the values shown in Table 8-9. (Use high-impedance 10:1 probes.)

Table 8-9. Detector Voltages

	Full Leveled +13 dBm	**Full Unleveled **+20 dBm**
A4P1-21	−150 to −200 mV	−300 to −400 mV

If the detector is working and the Detector Selection Switch is suspected, sweep the full band and monitor TP15 for the voltages seen at the selected input of U6B.

If the EXT/MTR ALC INPUT circuits are suspected, select the desired mode and supply a test signal (low-level DC or sine wave) in the front panel BNC connector, and trace it through U6B at A4TP15.

NOTE

Remove any tape applied to edge connector pins in the previous procedure.

Detector Leg Ⓓ Ⓔ

The "Detector Leg" of the ALC loop includes components between the Detector Selection Switch and the Error Summing Amplifier U3D.

Before troubleshooting the Detector Leg, be sure the Detector and Detector Selection Switch are working correctly. See above.

The Detector Leg can be effectively tested by using the Open Loop method of troubleshooting. This procedure utilizes the external leveling mode **EXT** by supplying an external DC voltage or sine wave to the EXT/MTR ALC INPUT connector. This method breaks the ALC loop and allows waveforms to be checked against known test signals. See Figure 8-33 (above the schematic diagram).

Modulator Leg Ⓖ Ⓘ

The "Modulator Leg" includes the Error Sample & Hold and the Main ALC Amp.

U3D is a non-inverting unity-gain summing amplifier. Under leveled conditions, both TP4 and TP7 should be nearly 0.0 Vdc. Under any conditions, TP4 and TP7 should be at the same voltage. If not, suspect U3D, Q3, or the Sample & Hold Driver.

U11 forms an inverting integrator. When TP7 is positive, TP6 should be at −0.6 Vdc. If not, suspect U2D or U11. When TP7 is negative, TP6 should be at +7.5 Vdc. If this is not the case, suspect U11.

- The following procedure can be used to check U3D and U11:

  1. Set power for −2 dBm at any CW frequency.

  2. Press 83522A **EXT** ALC.

  3. Ground A4TP11.

  4. To check U3D, monitor TP4 and TP7 while adjusting the EXT/MTR ALC **CAL** knob between the extremes of its range. Both TP4 and TP7 should vary between approximately +0.5 and −0.5 Vdc.

  5. Verify U11 by adjusting the **CAL** knob as described above and monitoring TP6. Since U11 is an integrator, TP6 should saturate and clamp (due to VR4) at −0.6 Vdc and +7.5 Vdc, respectively.

Further troubleshooting of the Modulator Leg can be continued by following the Open Loop procedure outlined in Figure 8-33 and checking for the waveforms provided in Figure 8-34.

Modulator Driver (K)

The PIN Mod 0 Driver provides the voltage-to-current conversion and current gain needed to drive the modulator. As the voltage increases at TP6 so does the current to the Modulator, shunting more RF energy to ground and allowing less to pass through. Since the modulator is essentially current-controlled, the voltages measured at TP8 and P1-44 do not vary much over a wide range of modulator attenuations.

The PIN Mod 0 Driver is an emitter-follower followed by a common-base stage, with two diodes in between. Check the biases and base-emitter voltages to check for damaged transistors.

- To establish a bias level for the PIN Mod 0 Driver, TP6 can be forced high (+7.5 Vdc) by pressing 8350A CW and selecting any CW frequency. Select EXT ALC, and enter an RF power level of −2 dBm via front panel controls. Ground A4TP11. Rotate the EXT/MTR ALC CAL knob fully counter-clockwise to set a signal level of approximately +7.5 Vdc at TP6.

Modulator/Mixer A17, A13

The internal modulator for this plug-in is housed in a combination microcircuit package (A17 Modulator/Mixer). Figure 8-28 provides a simplified schematic for this positive-bias shunt-type attenuators. As more current is supplied through the modulator bias pin, the harder the shunt diode turns on, sinking more RF power to ground and allowing less to reach the front panel.

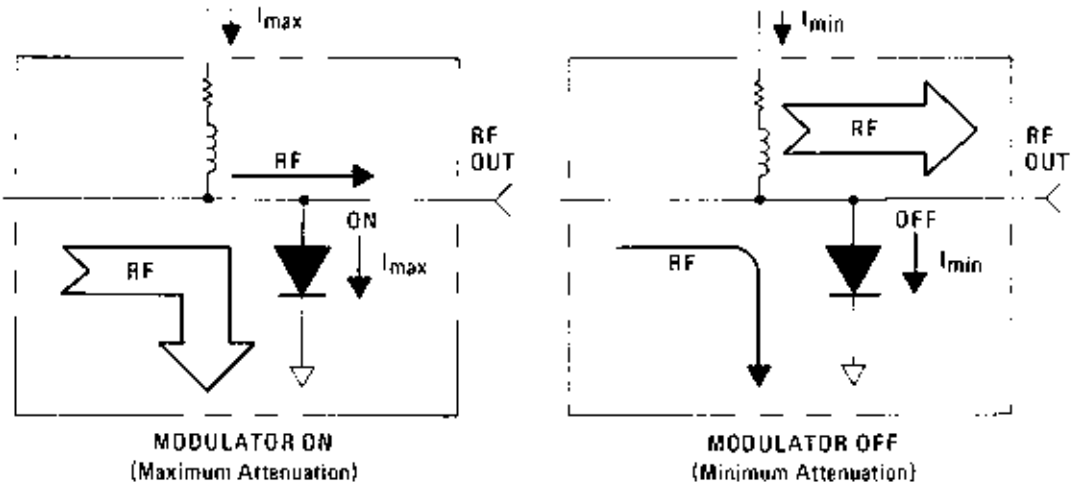


Figure 8-28. Simplified Modulator Schematic

The modulator is checked simply by noting whether the actual RF attenuation is appropriate to the modulation bias present:

NOTE

Turn off line power before removing or installing any assembly.

- If low or no RF power is observed, remove all modulator bias current simply by removing the A4 assembly from the motherboard. With no bias current, the RF power should pass through the modulator unhindered. If this is not the case, check the modulator diode as follows:

  1. Select 83522A **EXT** ALC. Enter −2 dBm RF power, and select a CW frequency at any point in the band. Ground A4TP11. Rotate the EXT/MTR ALC CAL knob fully clockwise to set TP6 to −0.6 Vdc, essentially removing bias from the modulator. Check TP8 for −10 Vdc. If this is not the case, isolate the modulator from the drive circuitry by applying a piece of cellophane tape to the pin edge connection (P1−44). If TP8 now measures −10 Vdc, the modulator diode is probably shorted. If the test point still does not achieve −10 Vdc, suspect the blanking circuitry, U9B and Q9.

NOTE

Remove any tape applied to the pin edge connector in the previous procedure.

If the modulator appears to be functioning properly, check the following RF levels with a power meter or spectrum analyzer. When checking power levels internal to the RF signal path, ensure that all critical ports are terminated in 50 ohms.

  2. If power is low, check the RF level directly out of A12 YO. Refer to the RF Schematic Diagram at the end of Section VIII for the proper levels. Measure the RF levels around A17 Mod/Mixer. With no modulation, approximately +13 dBm should be measured at the input of A17, with approximately −10 dBm at the output. If no output is measured, make sure the A16 Cavity Oscillator output is at least +8 dBm.

- If maximum unleveled RF power is observed, attempt to achieve maximum attenuation (minimum RF transmitted). Select 83522A **EXT** ALC. Enter −2 dBm RF power, and select a CW frequency anywhere in the band. Ground A4TP11. Rotate the EXT/MTR ALC CAL knob fully counter-clockwise. The voltage level at TP6 should be +7.5 Vdc. The voltage levels at the output of the PIN Mod 0 Drivers (P1-44) should be approximately +0.6 Vdc to +0.8 Vdc.

  1. If the voltages are significantly higher than this, the modulator diode is probably open.

  2. Check TP8 for approximately +2.0 Vdc. The difference between the test point and the pin-edge connector gives an indication of how much current is flowing to the modulator.

A4

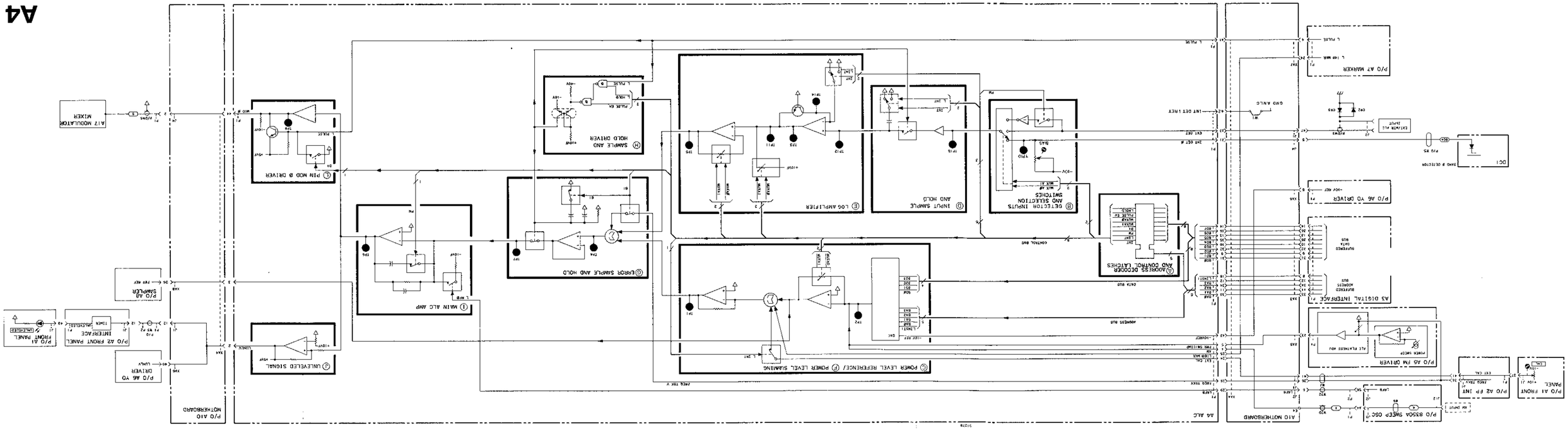


Figure 8-29. A4 ALC Block Diagram

A5 FM DRIVER, CIRCUIT DESCRIPTION

The A5 FM Driver is divided into three major sections: the YIG Main Coil FM Driver, the YIG FM Coil Driver, and the ALC Flatness Adjustments and Power Sweep circuits for the A4 ALC assembly.

The FM input signal from the rear panel of the 8350A Sweep Oscillator provides the input to both the YIG Main Coil and FM Coil Driver circuits. For low frequency FM inputs, the Main Coil Driver scales and buffers the FM signal to produce an output that is summed with the tuning voltage for the YIG main coil on the A6 YO Driver. Thus, the Main Coil Driver output is an extra tuning voltage input to the YIG Oscillator and may be used for phase locking, frequency offsetting, or low frequency FM applications (where up to 75 MHz deviations are required). The FM Coil Driver scales and buffers the FM input signal to produce the current drive for the FM coil in the YIG oscillator for smaller deviation but wideband (up to 10 MHz) FM applications. Relay switches provide the option of selectable sensitivities of −6 or −20 MHz/Volt and/or DC coupling the FM input to the FM Coil Driver circuits. In the DC coupling mode, the main coil driver is shut off and the FM Coil Driver operates over the frequency range of DC to 10 MHz with −20 MHz/Volt sensitivity. The relay switches are controlled by the state of the Configuration Switch on the A3 Digital Interface board.

The ALC Flatness Adjustments circuit is used to flatten output power versus frequency by introducing an error voltage into the ALC reference channel. The Power Sweep circuit is activated by the front panel POWER SWEEP pushbutton and produces a scaled ramp that is summed with the ALC reference voltage causing the output power to increase level versus sweep (the amount of which is selected on the front panel).

YIG Main Coil FM Driver (B)(E)

The YIG Main Coil FM Driver scales and buffers the 8350A rear panel FM input signal for FM frequencies between DC and 700 Hz to produce an output which is summed with the tuning voltage for the YIG main coil on the A6 YO Driver board. Low Frequency Amplifier/Filter and Low Frequency Sensitivity Select circuits make up the YIG Main Coil FM Driver. The FM input signal is filtered by 700 Hz low pass filter R2/C1 and buffered by difference amplifier U7A. The gain of U7A is approximately 1.4. The output of U7A drives the Low Frequency Sensitivity Select/Amplifier circuits. Relay K2 is used to control the overall gain of inverting amplifier U7B by changing the value of the input resistance. Relay K2 is either open or closed (shorting resistor R8) according to the state of control line 6 MHz/V SEL (1 = −6 MHz/Volt, 0 = −20 MHz/Volt sensitivity) The state of control line 6 MHz/V SEL is determined by the position of the Configuration Switch on the A3 Digital Interface board. The overall gain for the main coil driver is approximately 0.239 with −6 MHz/Volt sensitivity selected (K2 open) and 0.807 with −20 MHz/Volt sensitivity selected (K2 closed). The output of U7B (TP3) is summed directly with main coil tuning voltage on the A6 YO Driver board. The YIG main coil driver is shut off with analog switch U3D when the DC coupling mode is selected (on the A3 board Configuration Switch) causing control line L LO FM OFF (Low = Low Frequency FM OFF) to be true.

YIG FM Coil Driver (D)(F)(H)

The YIG FM Coil Driver scales and buffers the 8350A rear panel FM input for frequencies between DC and 10 MHz to produce an output current that drives the YIG FM coil. The FM Coil Driver is made up of a high pass filter, buffers Q5A and Q5B, video amplifier U10, operational amplifier U19, and unity gain follower U20. The high pass filter is made up of capacitors C2 through C6 and resistors R11 and R12. The filter has a 3 dB cutoff frequency of about 700 Hz. When the FM Driver is configured for the crossover mode as determined by the position of the Configuration Switch on the A3 Digital Interface board, the FM Coil Driver passes FM input signals above 700 Hz and the low pass filter in the Main Coil driver circuits will pass signals below 700 Hz. If the DC coupling mode is selected, the Main Coil driver is shut off and control line L DC COUPLE is true, activating relay K1. This shorts the high pass filter network, and the FM driver is active for frequencies of DC to 10 MHz.

Selectable sensitivities of −6 MHz/Volt and −20 MHz/Volt are available and determined by the state of control line 6 MHz/V SEL (1 = −6 MHz/V, 0 = −20 MHz/V). When 6 MHz/V SEL is high, relay K2 is open and the FM input is scaled by a resistive divider made up of R11 and R12. When 6 MHz/V SEL is low, relay K2 is activated, shorting capacitors C4, C5, C6 and resistor R11. The combination of C2, C3, and R12 still form a high pass filter with a cutoff of 700 Hz. Note that in the DC Coupled mode the sensitivity is always −20 MHz/Volt.

The output of the filter network is limited to about ±3 Vdc with a network made up of VR1, VR2, R14, R15, CR3, and CR4. Q5A and Q5B are connected as emitter followers and buffer the output of the filter network to video amplifier U10. Analog switch U11 is always set to switch position zero. Frequency response shaping to compensate for the roll-off versus frequency of the FM coil is produced by the network made up of C11, C12, C14, R21, R22, R23, R75, and L1 connected across pins 9 and 4 of U10. This network is actually in the emitter of the input differential amplifier of U10 producing greater gain with decreasing impedance. Figure 8-36 shows the approximate response versus frequency of the YIG FM coil and the compensation network. Adjustments R19 (FM OFFSET), R75 (H1), and C14 (LO) adjust the shape of the compensation network response.

The differential output of U10 drives the wideband Output Current Driver, U19 and U20. The voltage difference between the outputs of U10 at pins 6 and 7 is converted to a proportional current which directly drives the YIG FM coil. The overall voltage gain of the Output Current Driver is about 2.0 (between U10 pin 6 and TP6). Resistive divider R30 through R32 sets the FM coil drive scale factor.

Address Decoder (A)

Address Decoder U18 generates two control lines (LEN 4 and LEN 4) by decoding the state of address lines BA0 through BA3 and control line L INST L. LEN 4 (Low Enable 4) loads data into the Control Latch and LEN 5 (Low Enable 5) loads data into the Power Sweep DAC.

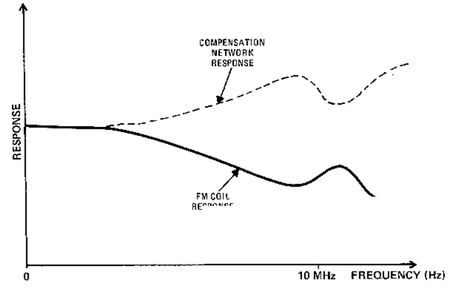


Figure 8-36. Plot of FM Coil Response Versus Modulation Frequency

Control Latches (C)

Control Latch, U16, stores the state of four control lines that are used to set the signal path and amplification factor of the FM input signal. The state of the control lines is determined by the position of switches 5 and 6 of the Configuration Switch on the A3 Digital Interface board. The control lines are loaded into U16 from Data bus lines BD2 through BD5 when the LEN 4 signal from U18 makes a low to high transition.

ALC Flatness Adjustments (I)

The purpose of the ALC Flatness Adjustment circuit is to produce an RF OUTPUT signal that is as flat as possible across the entire frequency band. The input of the ALC flatness circuit is a 0 to 6 Volt ramp (in full sweep) labeled FREQ TRK V (Frequency Tracking Voltage). This ramp is dependent on the frequency START and STOP settings, so it will always be at least a portion of the 0 to 6 Volt range.

The FREQ TRK V ramp is applied to four parallel circuits, each one adjusted to take affect at a different frequency (i.e., voltage threshold of FREQ TRK V) as the sweep progresses from START to STOP. Since the four circuits are identical (Q1, Q2, Q3, Q4), only the Q1 circuit will be discussed. Q1A is connected as a diode, is always conducting, and is in the circuit for temperature compensation of Q1B. The setting of adjustment BP1 (R34) determines at what point on the input ramp Q1B will conduct. When the summing point at the junction of U2C and R33 is at zero Volts or greater, Q1B will conduct. The junction of resistors U1B and U1A form another summing point. U1B applies a positive-going ramp from Q1B to this summing point, and a negative-going ramp comes through U1A from the output of U14C. Slope adjustment SLI adjusts the amount of negative-going ramp contributed to the summing junction through U1A, and thus determines the resultant contribution of the Q1 circuit to the input of U14A. That is, the resultant signal may be either a positive-going ramp or a negative-going ramp as required to make the RF OUTPUT signal flat over that frequency segment.

The composite correction signal from the four flatness adjustment circuits (Q1 through Q4) are summed at the input of U14A then are applied to the Power Level Reference in the ALC circuit. TP1 shows this composite correction signal. Overall tilt is adjusted by SLP (Slope) adjustment R48.

Power Sweep (H)

When POWER SWEEP mode is selected at the front panel, LEN 4 (Low Enable 4ALC generated by U18, enabling U17 on. This allows power sweep data from

signal path of the YSW voltage sweep signal (0 to +10V), is through the selected gain resistors in U17 to input pin 6 of U14B. The feedback resistor for U14B is also within U17 and is internally connected to the input of the amplifier stage. The output of U14B is summed at the input of U14A with the ALC flatness signal. The output of this entire circuit is then sent to the Power Level Reference in the ALC circuit.

When the plug-in front panel SLOPE key is depressed, data lines BD0 through BD7 redefine the gain of the Power Sweep circuit to compensate the slope of the RF output in dB/GHz.

TROUBLESHOOTING

For troubleshooting purposes, the A5 FM Driver is divided into three groups:

- YIG Main Coil FM Driver and YIG FM Coil Driver circuits.
- FM Configuration Control circuits.
- Power Sweep and ALC Flatness Adjustment circuits.

YIG Main Coil FM Driver and YIG FM Coil Driver Troubleshooting

The most likely indication of a failure in these circuits is unpredictable or no FM operation. A failure in these circuits can also cause excessive residual FM or frequency offset.

Troubleshooting waveforms at various points within the FM driver circuits for FM input frequencies of 100 Hz, 700 Hz, 1 MHz, and 10 MHz are given in Figure 8-42. The waveforms are arranged horizontally by test point and vertically by the FM input frequency. Figure 8-41 shows the test setup required to obtain the waveforms.

NOTE

Before altering the switch settings on A3S1, note the present configuration. Return the switches to their original status after troubleshooting.

A4

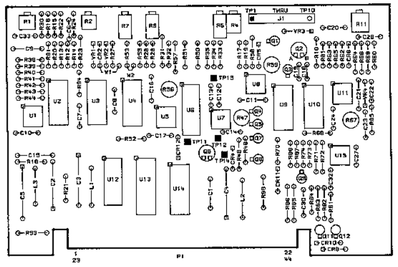


Figure 8-30. A4 ALC, Component Locations

NOTES

1. THE FOLLOWING KEY ENTRIES PROVIDE FRONT PANEL ACCESS FOR A DATA WRITE/READ OPERATION TO/FROM THE ADDRESSED LOCATION:

FUNCTION	KEY ENTRY
*Hex Address Entry	SHIFT 0 0 (enter hex address)
Hex Data WRITE	M2 (enter data: two hex digits)
Hex Data READ	M3
Hex Data Rotation Write	M4
Hex Addressed Fast Read	M5

*TO ADDRESS A DIFFERENT LOCATION, PRESS M1 AND ENTER THE NEW ADDRESS, OR USE THE INCREMENT KEYS ◆ ◆ TO STEP TO THE NEW ADDRESS.
TO PREVENT THE MICROPROCESSOR FROM SERVICING THE RETRACE INTERRUPT, PRESS 8350A CW .

Table 8-10. Leveling Control Lines

Data Bus		Leveling Mode
Mux A1	Mux A0	
H	H	INT 0
H	L	INT 1
L	H	EXT DET
L	L	POWER METER

A4P1

PIN	SIGNAL	I/O	TO/FROM	BLOCK
1	EXT DET RET	IN	A10J1-43	M
23	EXT DET	IN	A10J1-47	B
2	L UNLVL	OUT	A9P1-40	J
			A10J1-12	
24	EXT CAL	IN	A10J1-41	F
3	PWR REF	OUT	A9P1-26	C
25	L1dBMKR	IN	A7P1-24	F
4	AM	IN	P1-A4	F
26	FREQTRKV	IN	A10J1-35	G
5	PWRSW/COMP	IN	A9P1-23	C
27	+5V	IN	A9P1-6,7	M
6			NOT USED	
28	−15V	IN	P2-28	M
7	+10V	IN	P1-8	M
29	L RFB	IN	P2-56	I
8	GND DIG			M
30	GND DIG			M
9	BD1	IN	A3P1-8	AC
31	BD0	IN	A3P1-31	AC
10	BD3	IN	A3P1-10	AC
32	BD2	IN	A3P1-32	AC
11	BA1	IN	A3P1-11	AC
33	BA0	IN	A3P1-33	AC
12	BA3	IN	A3P1-12	AC
34	BA2	IN	A3P1-34	AC
13	BD5	IN	A3P1-13	A
35	BD4	IN	A3P1-35	A
14	BD7	IN	A3P1-14	A
36	BD6	IN	A3P1-36	A
15	GND ANLG			M
37	GND ANLG			M
16			NOT USED	
38	+15V	IN	P2-29	M
17	−10V	IN	P1-12	M
39	−40V	IN	P1-11	M
18	L INST1	IN	A3P1-8	AC
40	DET REF	OUT	NC	C
19	MOD 1	OUT	NOT USED	
41	L PULSE	IN	A7P1-4	H L
20	INT DET 1	IN	NOT USED	B
42	INT DET RET	IN	NOT USED	M
21	INT DET 0	IN	J4-5	B
43	−10V REF	IN	A6P1-5	C
22	MOD DRIVE	OUT	NC	K
44	MOD 0	OUT	A10J4-2	L

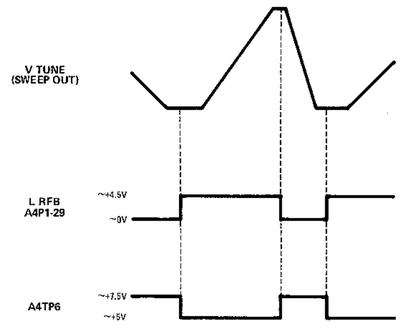


Figure 8-31. Retrace Blanking Waveform

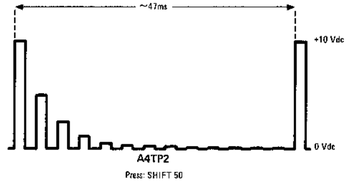
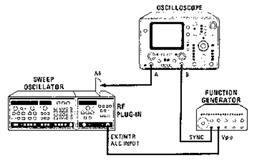


Figure 8-32. ALC DAC Test Waveform



Open Loop Procedure Test Setup

EQUIPMENT:

Function Generator	HP 3312A
Oscilloscope	HP 1740A

PROCEDURE:

1. Press 8350A INSTR PRESET .
2. Press 83525A EXT ALC.
3. Adjust Function Generator output for a 50 mV p−p sine wave at 500 Hz. Adjust the OFFSET knob for −25 mVdc.
4. Connect Function Generator output to EXT/MTR ALC connector.
5. Set oscilloscope DISPLAY to A and TRIGGER COMP to B. Check for the waveforms shown in Figure 8-34.

NOTE

The HP 3312 OFFSET knob may have to be adjusted slightly to produce the waveforms given in Figure 8-34. If the EXT/MTR ALC input goes positive, the Log Amp will saturate.

Adjustment of the EXT/MTR ALC CAL knob will affect the waveforms at TP4, TP7, and TP6. Adjust the CAL knob until these waveforms are obtained.

Slight differences may be noted between the waveforms shown in Figure 8-34 and those obtained on individual ALC assemblies. This is due to the many adjustments on the A4 assembly.

Figure 8-33. Open Loop Procedure

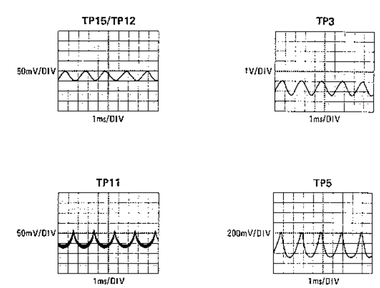


Figure 8-34. Open Loop Waveforms

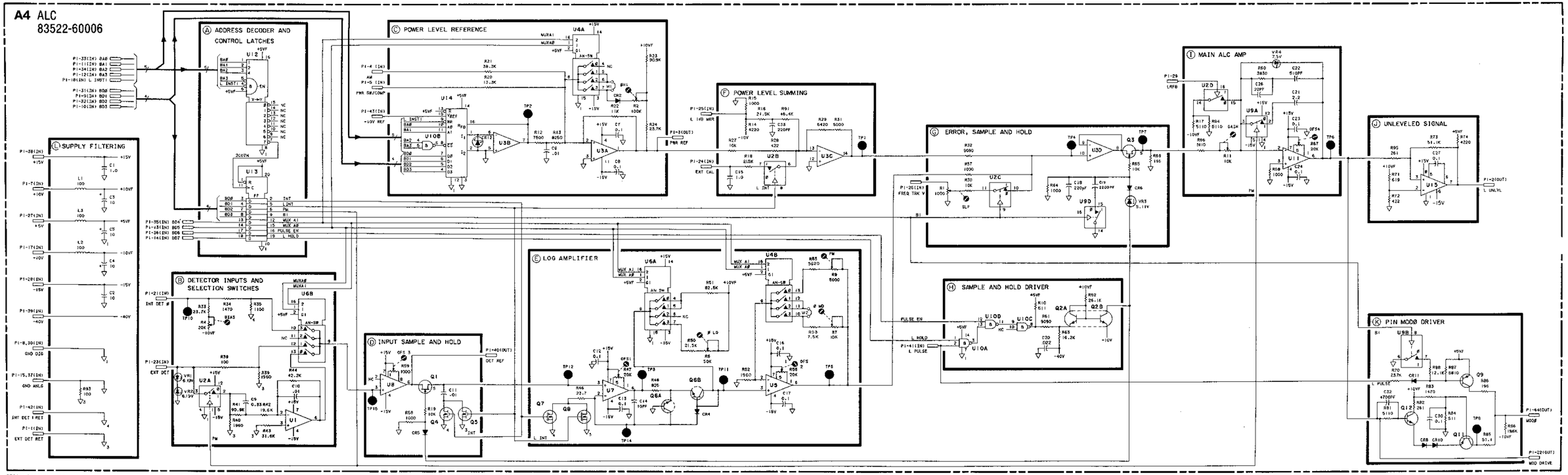


Figure 8-35. A4 ALC, Schematic Diagram

Prior to performing the test procedure, preset the A3S1 Configuration switch sections 5 and 6 to the closed (0) position. Several of the troubleshooting waveforms require different switch settings. A description of each switch setting follows.

- For **−6 MHz/V Sensitivity** − set A3S1 section 5 to the open (1) position.
- For **−20 MHz/V Sensitivity** − set A3S1 section 5 to the closed (0) position.
- For **DC Coupled mode** − set A3S1 section 6 to the open (1) position.
- For **Cross-Over Coupled mode** − set A3S1 section 6 to the closed (0) position.

NOTE

The 8350A front panel INSTR PRESET pushbutton must be pressed after each switch position change in order for the selection mode to take effect.

1. Adjust the function generator frequency and amplitude controls to obtain one of the waveforms in the first column (TP11) of Figure 8-42.
2. Verify the remaining waveforms in the corresponding row.

FM Configuration Control Circuits Troubleshooting

The FM configuration control circuits include the Address Decoder, Control Latches, relays K1 and K2, and analog switches U3D and U11. Incorrect or no operation in a specific configuration mode is the most likely result of a failure in these circuits.The troubleshooting procedure for these circuits uses several of the 8350A Sweep Oscillator operator initiated self tests. Separate tests for each section of the configuration control circuits are provided in the following paragraphs.

Address Decoder. Check proper Address Decoder operation by performing a Minor Address Decoder Self Test.

On the 8350A, enter:

SHIFT 5 4	Minor Address Decoder Test

Check the Address Decoder outputs LEN 4 and LEN 5 as shown in Figure 8-37.

Control Latches. Control latch U16 is checked by performing a hexadecimal data rotation write to U16, and then checking the outputs for the waveforms shown in Figure 8-2. The oscilloscope should be triggered from U16 pin 15.

Exercise U16 with Hex Data Rotation Write. Enter:

SHIFT 0 0	Enters Hex Data command
2 GHz s 0 4	Address location 2C04 (U16)
M4	Hex Data Rotation Write

Check the outputs of U16 against waveforms shown in Figure 8-2.

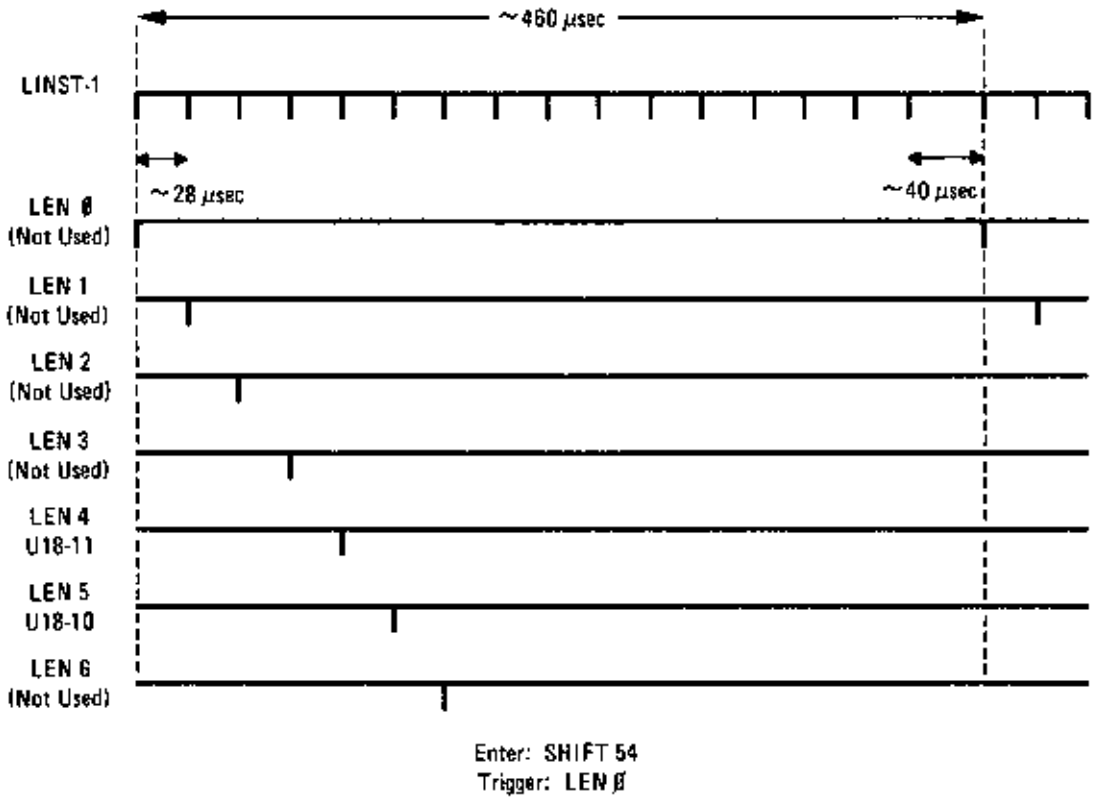


Figure 8-37. A5 Address Decoder Timing Waveforms

Relays K1 and K2. A known FM input is applied and the waveform at TP4 is monitored. The Hex Data Write feature of the 8350A is used to control relays K1 and K2. Connect equipment as shown in Figure 8-41. Adjust the function generator for a 500 Hz 1 V peak-to-peak sine wave output with a +0.5 Vdc offset (use function generator offset control).

To check relay K1, enter on the 8350A:

SHIFT 0 0	Enters Hex Data command
2 GHz s 0 4	Address location 2C04 (U16)
M2 . 8	Hex Data Write A8

Relay K1 should be open. Verify that there is a signal centered around 0 Vdc at TP4.

On the 8350A, enter:

M2 8 8	Hex Data Write 88

Relay K1 should now be closed. Verify that the signal at TP4 is offset from being centered around 0 Vdc.

To check relay K2, enter on the 8350A:

M2 BK SP 8	Hex Data Write F8

Relay K2 should be closed. Note the level of the signals at TP3 and TP4.

Open relay K2 by entering on the 8350A:

M2 dBm dB 0	Hex Data Write E8

Relay K2 should now be open. Verify that the level of the signals at TP3 and TP4 is less than previously noted.

Analog Switches U3D and U11. The analog switches are checked by using the Hex Data Write feature of the 8350A to control the switches. A known FM input is applied and switch operation is verified.

Connect equipment as shown in Figure 8-41. Adjust the function generator for a 500 Hz 1V peak-to-peak sine wave output.

On the 8350A, enter:

SHIFT 0 0	Enters the Hex Data command
2 GHz s 0 4	Address location 2C04 (U16)
M2 dBm dB 8	Hex Data Write E8

Analog switch U3D should be closed. Verify that there is a signal at TP3.

On the 8350A, enter:

M2 dBm dB 0	Hex Data Write E0

Analog switch U3D should be open. Verify that there is no signal at TP3.

On the 8350A, enter:

M2 dBm dB 8	Hex Data Write E8

Analog switch U11 should be set to the zero position. Verify that a signal is present at TP6.

On the 8350A, enter:

M2 dBm dB GHz s	Hex Data Write EC

Analog switch U11 should be set to the one position. Verify that no signal is present at TP6.

Power Sweep/ALC Adjustments Troubleshooting

The most likely indication of a failure in these circuits is either incorrect or no operation of the Power Sweep function or inability to adjust the output power flatness. The Power Sweep DAC U17 is exercised by initiating the Power Sweep DAC self test, and the DAC output is checked at TP8. On the 8350A, enter:

SHIFT 5 1	Initiate Power Sweep DAC Self Test

Verify the waveform at TP8 corresponds with the waveform in Figure 8-38.

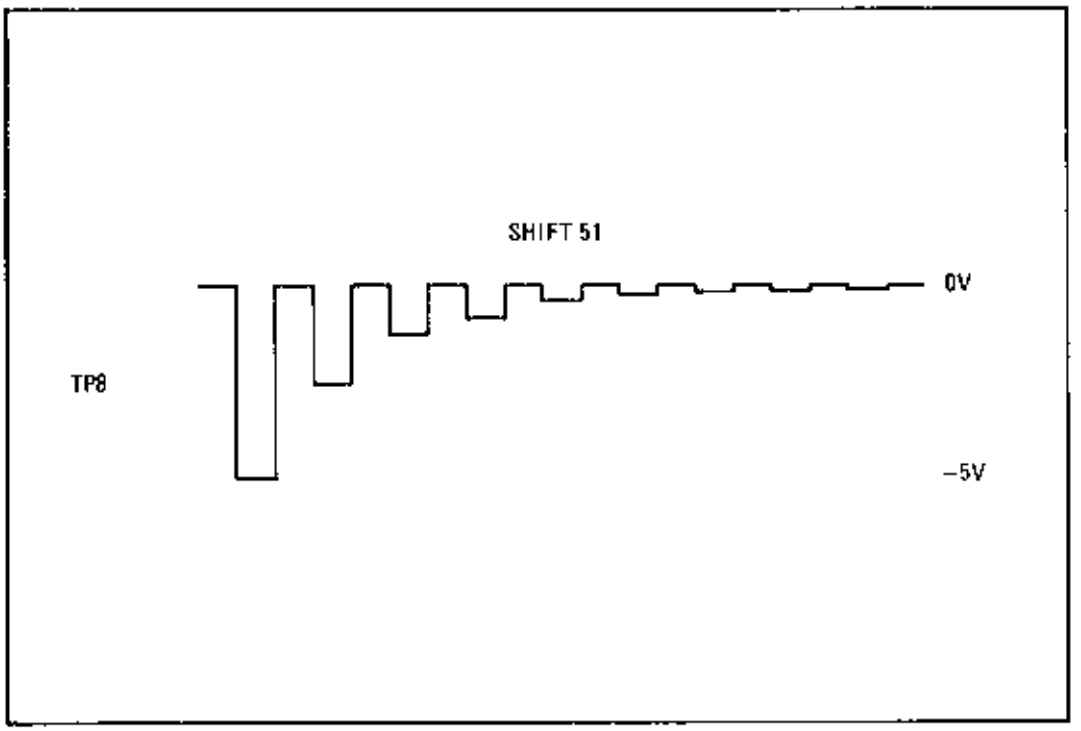


Figure 8-38. Power Sweep DAC Self Test Waveform

A5

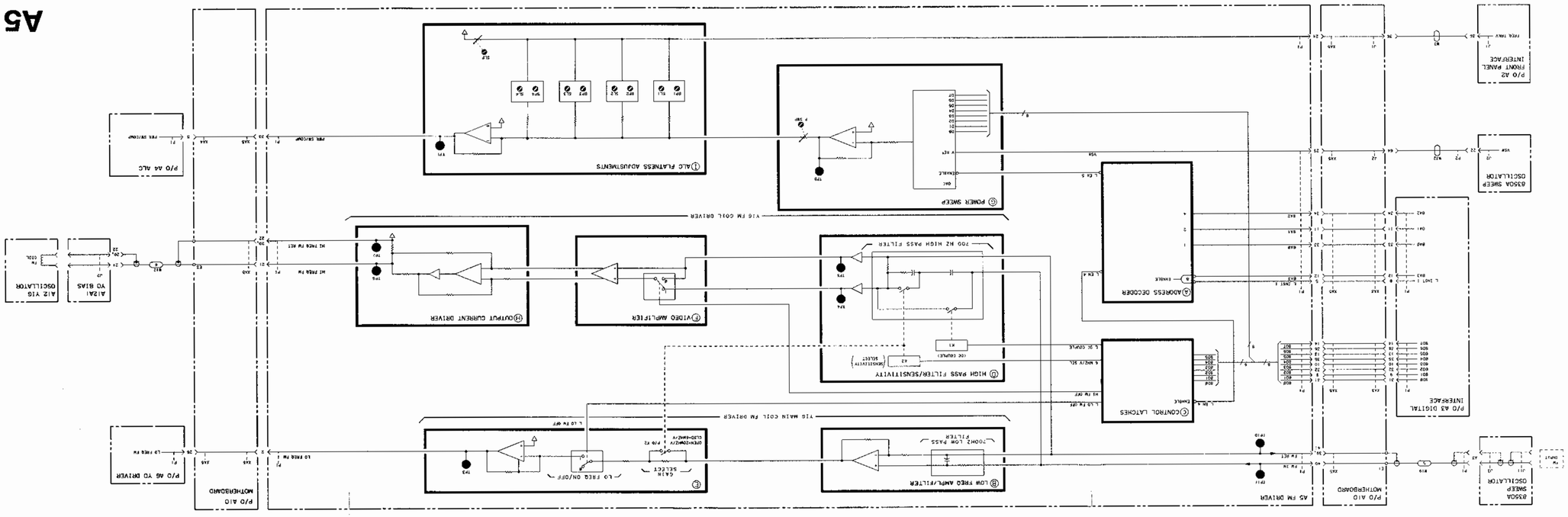


Figure 8-39. A5 FM Driver, Block Diagram

A6 YO DRIVER/A9 REFERENCE RESISTOR, CIRCUIT DESCRIPTION

NOTE

All reference designators refer to the A6 assembly unless otherwise noted.

GENERAL

The A6 YO Driver assembly converts the tuning voltage from the 8350A mainframe into a drive current. The A9 Ref Resistor assembly provides the current driver to control the frequency of the YIG Oscillator (YO). (The A6 y also initiates band-switch sequence in multi-band plug-ins.)

ying Digital-to-Analog Converters (DACs) scale and offset the buffered voltage to the frequency end-points of the plug-in. A summing amplifier lay compensation, low frequency external FM, and the FREQ CAL offset from the front panel. The resultant waveform at TP14 is then converted to a current-drive for the YO's Main Coil. Sweep control circuitry interrupts the microprocessor at the end of each sweep. (Band-switch circuitry is disabled in the 83522A.)

Tuning Voltage Buffer Amplifier (B)

U10 receives the tuning voltage from the 8350A mainframe and buffers it for use on the rest of the board. The circuit is arranged as a differential amplifier, with the tuning signal appearing at the inverting input and the cable shield at the non-inverting terminal. This provides good common mode rejection to eliminate noise picked up on the cable. The waveform at TP4 is an inverted ramp, ranging from 0 to −10V for sweeping the full frequency range of the plug-in. See Figure 8-50.

Scaled Voltage Tune DAC (D)
Offset DAC (F)

U9 is a 12-bit multiplying DAC, which scales the tuning voltage according to the binary pattern loaded at its inputs. Inverting amplifier U13 and emitter-follower Q3 are included in the feedback path to provide the current gain needed to drive later stages. CR1 prevents transients from damaging the DAC during turn-on. C1, along with the DAC's internal feedback resistor, determine the bandwidth of the circuit. The waveform at TP1 is a scaled ramp, with a maximum range of 0 to +10Vdc. See Figure 8-50.

U19 is a 12-bit multiplying DAC which scales a stable −10V REF voltage according to the binary pattern loaded at its inputs. Inverting amplifier U14 works with the DAC's internal feedback resistor to provide a programmable offset voltage between 0 and +10Vdc at TP2. See Figure 8-50. CR2 protects the DAC from turn-on transients. C11 and the DAC's internal feedback resistor determine the bandwidth of the circuit.

SCVTUNE and OFFSET DACs function together to determine the frequency of the YIG oscillator. The Offset DAC determines the start frequency while the Scaling DAC sets the gain of U16 so that SCVTUNE determines the high end frequency. For full-band sweeps, the entire 0 to −10 Volt VTUNE is scaled and offset to sweep the YO from 3.8I to 6.2 GHz. The YO output is ten heterodyned with 3.8 GHz from the Fixed Cavity Oscillator for a full-band range of 0.01 to 2.4 GHz.

Input Data Latches (C)

Four octal latches store various signals including the digital data for the Scaling (D) and Offset (F) DACs, and the control signals for the Sweep Control/Interrupt Logic circuit (E). Each latch is clocked by a separate line from the Address Decoder to store the byte of data appearing on the Data Bus.

U8 stores the 8 least significant bits (S0 through S7) for the Scaling DAC (U9). The remaining four bits (S8 through S11) come from half of U13. Similarly, the least significant bits (O0 through O7) for the Offset DAC come from U18, with the remaining four (O8 through O11) coming from the other half of U13. The 8350A microprocessor multiplexes the two numbers so that they can be loaded in three bytes.

U22 is a control latch which stores commands from the 8350A for the control lines used on the A6 YO Driver assembly. (Several of these signals are associated with band-switching circuitry used in multi-band plug-ins and therefore are not used in this application.) The command byte is latched into U22 when LEN3 pulses low. Refer to the Summing Amplifier, YO Coil Current Source, and Sweep Control/Interrupt Logic sections for detailed descriptions of these control lines.

LRFBRQ is not used in the 83522A.

+20V Tracking Amplifier (G)

Inverting amplifier U11 monitors the +20V line (TP13/15) used to supply current to the YIG Oscillator. If the +20V supply becomes loaded down or drifts, the YO Main Coil current and, consequently, the frequency will try to change. However, U11 senses any drift in the +20V FREQ REF line, and provides a correction signal so that the resultant YO DRIVE Voltage (TP14) is compensated for the drift.

Summing Amplifier (I)

U16 provides the summing point for the scaled tuning and offset voltages, and provides a drive voltage (YO DRIVE V) for the Current Driver. Several correction signals are summed at this junction:

SC V TUNE provides the scaled ramp portion of the YO DRIVE Voltage. R11, 'G', fine-tunes the range of the scaling DAC (D).

OFFSET adjusts the YO DRIVE Voltage so that the YO Coil is driven between the proper end points, as determined by the front panel controls. R30, 'OFS', fine-tunes the range of the Offset DAC (F).

SUPPLY VOLTAGE CORRECTION provides a compensation signal, from the +20V Tracking Amplifier, to offset changes in the reference supply.

DLY COMP, from the A7 Marker assembly, is added to correct for lags in the response time of the YIG Oscillator. This compensation is derived from SC V TUNE (D).

FREQ CAL (from the A1/A2 Front Panel) is summed in through U26. (The BAND 0 line from U22 (C) is held high in the 8322A.) This offset corrects for errors in the Fixed Cavity and YIG Oscillator frequencies.

LO FREQ FM sums low frequency components of external FM signals onto the drive voltage when crossover coupling of the FM signal is selected. (Configuration switch A3S1 provides this adjustment. Refer to the A3 Service Sheet for further details.) Due to the response time limitations of the YIG Oscillator's main coil, only frequencies below 700 Hz are passed from the A5 FM Driver assembly to the A6 YO assembly.

−10V REF and R25 'ZRO' adjust for gain and offset inaccuracies between U11 (G) and summing amplifier U16.

−10V Reference (J)

U23 contains a low-noise 6.95V zener diode to provide a stable voltage reference for the rest of the plug-in. The package includes an internal heater to control its temperature and improve its stability. R19 and C7 filter the reference voltage to the non-inverting terminal of differential amplifier U20. R21, '−10', adjusts the overall gain for exactly −10V at TP3. C8 limits the high-frequency gain of the system to reduce noise. R24 provides the bias current for the zener diode from the −10V REF output. R23, with filtering capacitor C9, increases the current drive capability of the −10V REF.

Sweep Control/Interrupt Logic (E)

NOTE

Most of the signals discussed in this section are illustrated in Figure 8-50.

Band-switch circuitry is disabled in the 83522A. The L BSE line from U22 is held high by microprocessor control, thereby grounding the input to comparator U5. This effectively disables U5, U21A, and U17A.

In the 83522A, the SS HOLD line is also deactivated by microprocessor control, disabling U12A and U12B. However, L SSRQ (Low=Stop Sweep Request) and L BPRQ (Low=Blanking Pulse Request) are wire-ored signals and may appear active at the output, via several other sources.

End of Sweep Interrupt circuitry interrupts the microprocessor at the beginning and end of each sweep. Each time LRTS (Low=Retrace Strobe) changes from high to low, or low to high, U21C pulses high. (Pin 9 of U21C is prevented from tracking pin 10 by C16. Consequently, the output of EXOR U21C will pulse high everytime LRTS changes states.) Each pulse from U21C clocks flip-flop U17B. The noninverting output of U17B pulls LSIRQ low and requests microprocessor attention. LRTS is read through U7 to determine whether the forward sweep is beginning (LRTS=High) or ending (LRTS=Low). U17B is then reset by a control line from U22 and the microprocessor services the interrupt.

LRFBRQ is not used in the 83522A. It is activated only during bandswitching in multi-band plug-ins.

Frequency Cal Switches/Output Data Buffers (H)

DIP switches S1 and S2, with their corresponding data bus buffers, are used to digitally calibrate the low and high end frequencies. The data on these switches is read by the microprocessor during power-up and INSTR PRESET and used to calculate the settings for the Scale (D)and Offset (F) DACs. S1, with pull-up resistor package U1, is read through U3 when enabled by LEN4. S1 determines the value of the Offset DAC and calibrates the low end frequency. S2, with pull-up resistor package U2, is read through U4 when enabled by LEN5. This establishes the Scale DAC values, and calibrates the high end frequency. The ninth bits from S1 and S2 are read through U7.

S1 and S2 switch positions encode binary numbers to set up the Offset and Scaling DACs. Refer to the Frequency Accuracy adjustment procedure in Section V for instructions. Figure 8-51 illustrates the switch configurations.

The microprocessor reads U7 outputs each time it receives a retrace initiated interrupt to determine what action is required. LUNLVL, from the A4 ALC assembly, is read through U7. When the 8350A is under HP-IB control, the microprocessor alerts the controller to unleveled power conditions.

Supply Filtering (N)

Power supply circuitry provides eight different voltages for the A6 YO Driver and other assemblies. U27 provides a regulated +15V supply for the DACs. The other supplies use capacitive or LC filtering to reduce supply noise.

YO Coil Current Source (K)
YO Coil Current Driver A9 (M)

The YIG Coil Current Driver works with Reference Resistor A9R1 and YO Coil Driver A9Q1 to drive a current proportional to the drive voltage through the YIG's main tuning coil.

U24, Q1, Q2, and A9Q1 comprise a voltage-to-current converter and current driver for the YO's main coil. The non-inverting input of U24 receives the YO DRIVE Voltage signal. The inverting input of U24 monitors the voltage drop across reference resistor A9R1, which is directly proportional to the coil current. If the drive current is not tracking the drive voltage, U24 will produce an error voltage to correct the difference. Emitter-follower Q1 and common-emitter-stage Q2 provide the current gain needed to drive A9Q1. Q1 and Q2 emitter currents are also drawn through A9R1, and therefore, sensed by U24. VR1 and CR6 protect the current drive transistors by limiting voltage spikes due to sudden changes in the coil current. R42 helps to dampen ringing caused by the parasitic capacitance and the inductance of the YO coil.

When 8350A CW and 83522A CW FILTER are selected, LCW goes low, energizing relay K1. C14 filters out noise in the YIG coil current, reducing the residual FM noise in the CW mode.

CR7, CR3, CR4, and their associated factory-select resistors provide a three break-point compensation network to correct for non-linearities in the YO characteristics.

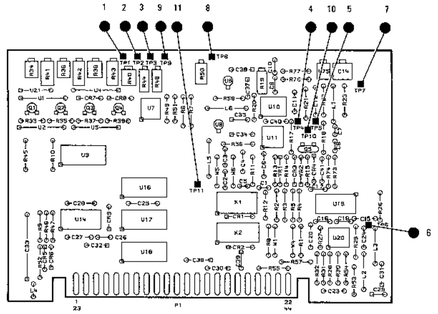


Figure 8-40. A5 Component Locations

NOTES

1. THE FOLLOWING KEY ENTRIES PROVIDE FRONT PANEL ACCESS FOR A DATA WRITE/READ OPERATION TO/FROM THE ADDRESSED LOCATION:

FUNCTION	KEY ENTRY
*Hex Address Entry	SHIFT 0 0 (enter hex address)
Hex Data WRITE	M2 (enter data: two hex digits)
Hex Data READ	M3
Hex Data Rotation Write	M4
Hex Addressed Fast Read	M5

*TO ADDRESS A DIFFERENT LOCATION, PRESS M1 AND ENTER THE NEW ADDRESS, OR USE THE INCREMENT KEYS ◆ ◆ TO STEP TO THE NEW ADDRESS.

A5P1

PIN	SIGNAL	I/O	TO/FROM	BLOCK
1 23	NC PWR SW/COMP	OUT	A4P1-5	I
2 24	LO FREQ FM FREQ TRK V	OUT IN	A6P1-25 A2J1-36	E I
3 25	NC VSW	IN	P2-64	G
4 26	NC NC			
5 27	L INST1 +5V	IN IN	A3P1-8 A3P1-6,7	A J
6 28	NC −15V	IN	P2-28	J
7 29	+10V NC	IN	P1-8	J
8 30	GND DIG GND DIG			J J
9 31	BD1 BD8	IN IN	A3P1-9 A3P1-31	C,G C,G
10 32	BD3 BD2	IN IN	A3P1-10 A3P1-32	C,G C,G
11 33	BA1 BA0	IN IN	A3P1-11 A3P1-33	A A
12 34	BA3 BA2	IN IN	A3P1-12 A3P1-34	A A
13 35	BD5 BD4	IN IN	A3P1-13 A3P1-35	C,G C,G
14 36	BD7 BD6	IN IN	A3P1-14 A3P1-36	G G
15 37	GND ANLG GND ANLG			NOT USED J
16 38	+20V +15V	IN IN	P1-7 P2-29	NOT USED J
17 39	−10V FM RET	IN IN	P1-13 P1-A3	J B
18 40	NC FM IN	IN	P1-A3	B
19 41	NC FM RET	IN	P1-A3	B
20 42	HI FREQ FM RET NC	OUT	A12A1J2	H
21 43	HI FREQ FM NC	OUT	A12A1J2	H
22 44	HI FREQ FM RET NC	OUT	A12A1J2	H

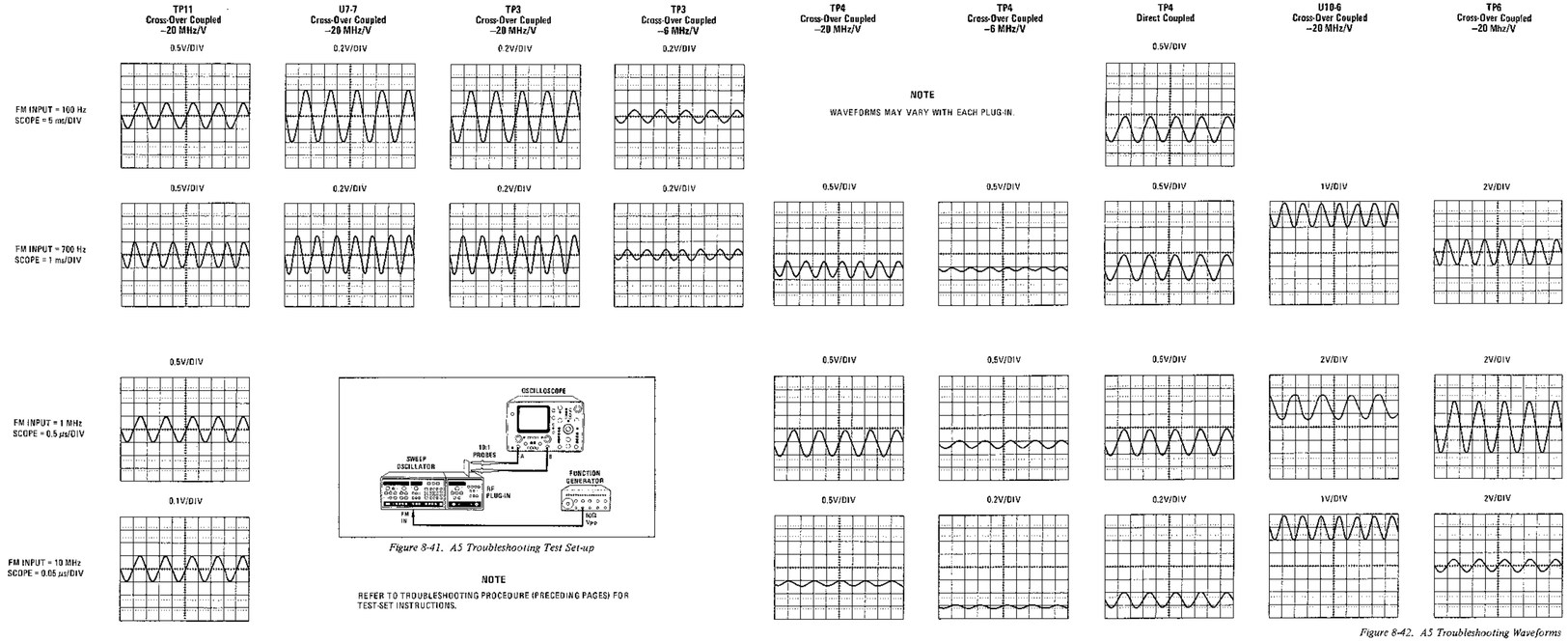
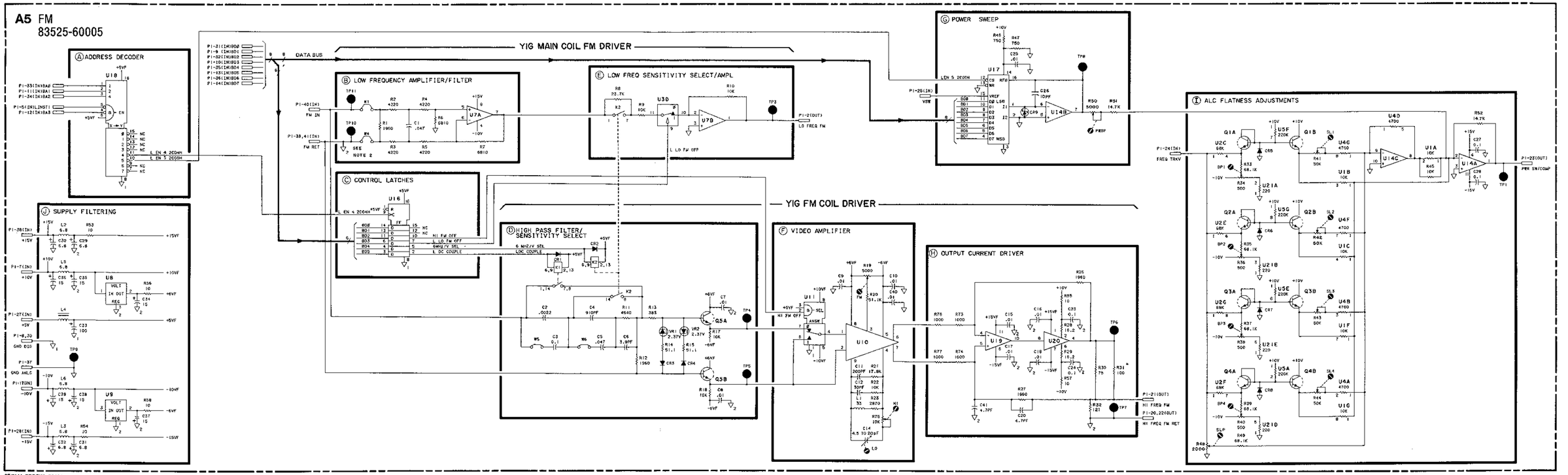


Figure 8-41. A5 Troubleshooting Test Set-up

NOTE

REFER TO TROUBLESHOOTING PROCEDURE (PRECEDING PAGES) FOR TEST-SET INSTRUCTIONS.

Figure 8-42. A5 Troubleshooting Waveforms



SERIAL PREFIX: 2040A

Figure 8-43. A5 FM DRiver, Schematic Diagram

NOTE

The values of the factory-select resistors are stamped on a label, attached to the RF casting. Matching resistor sets are supplied with replacement YOs and must be installed on the A6 YO assembly. The new label, indicating the replacement resistor values, should be attached to the RF casting.

If the A6 YO Driver Assembly is replaced, the shaping resistors from the defective board must be reinstalled in the new assembly.

NOTE

If the YO needs little or no compensation, some of the factory-select resistors may be omitted.

+5V Regulator A9 (L)

A9Q3 is a +5Vdc regulator mounted in a single package. It receives the +5V UNREG line (slightly more than 5V) from the mainframe, and regulates it for use in the plug-in RF components, A7 Marker, and A8 Sampler assemblies.

A6 YO DRIVER/A9 REFERENCE RESISTOR TROUBLESHOOTING

NOTE

All reference designators refer to the A6 assembly, unless otherwise noted.

The A6 YO Driver and A9 Reference Resistor assemblies are primarily responsible for controlling the RF output frequency. A failure in these assemblies usually results in large frequency errors that are independent of sweep time. (Frequency errors that change with sweep time are usually related to delay compensation. Refer to Service Sheet A7.) Frequency errors on the order of 500 MHz or less may be due to improper calibration. The problem may be relieved by performing the Frequency Accuracy adjustment in Section V.

General

Check that all power supply voltages are present. +20V (on the A6 assembly) and −40V (on the A12A1 assembly) supply the YO. Ensure that cable plugs are correctly seated over the correct jacks throughout the plug-in. With the line power off, remove and reseat the A6 assembly to assure good motherboard contact.

NOTE

Unless specifically stated otherwise, the troubleshooting waveforms and voltages described below occur when the plug-in is sweeping across its full range (INSTR PRESET conditions).

Sweep Circuitry

A failure in the sweep circuitry may cause the YIG to sweep between improper frequency endpoints, or, not sweep at all. If the YO Drive Voltage is missing, the instrument may toggle between two or more CW frequencies.

1. Check the YO DRIVE V (TP14) for the waveform shown in Figure 8-46. If this waveform is correct, then the Sweep and Interrupt circuits are working properly, and troubleshooting should continue with the YO Current Driver section below.

   a. If YO DRIVE V is incorrect, check BVTUNE (TP4) for the waveform shown in Figure 8-50. If it is missing or of the wrong amplitude, trace the problem back through the inputs of U10 (both should be close to 0 Vdc) to the sweep ramp output of the 8350A.

   b. If the waveform at TP14 appeared to be level-shifted, check −10 VREF (TP3) for −10 Vdc ±1 mV. Then, with the plug-in sweeping its entire range, check OFFSET (TP2) for approximately +9 Volts. If this signal is incorrect, select a CW frequency of 2.4 GHz and press **SHIFT** 5 2 . Check TP2 for a +0.4 to +9.2 Volt pulse. If this fails, check address decoding and the DAC latches using the Digital Control troubleshooting procedure described below.

2. If BVTUNE is correct, check SCVTUNE (TP1) against the waveform shown in Figure 8-50. If it appears to be bad, run the Scale DAC Test by setting a CW frequency of 8.4 GHz and pressing **SHIFT** 5 2 . Check that U9 pin 17 is at −10 Vdc. Then check TP1 for the waveform shown in Figure 8-53. If this fails, check address decoding and the DAC latches using the Digital Control troubleshooting below.

3. Check +20V FREQ REF (TP13) for +20 Vdc ±10 mV. If it is not, trace the supply voltage back to the 8350A. Then check that SUPPLY VOLTAGE CORRECTION (TP15) is at approximately −11.4 Vdc. If it is not, troubleshoot U11.

4. Finally, check that the summing junction, U16 pin 2, is at 0 Vdc. If it is not, troubleshoot U16.

YO Drive Circuits

1. Check +20V FREQ REF at TP13 for +20V ±10 mV. If it is not, troubleshoot back to the mainframe supply.

The circuitry surrounding U24 and A9Q1 is responsible for converting the YO DRIVE V to a drive current for the YO coil. A failure here will usually result in gross frequency errors.

2. Press **INSTR PRESET** to sweep the entire range of the plug-in. Check TP12 for the waveform shown in Figure 8-48. This represents the voltage (not the current) across the YO's main coil, and will give an indication as to whether current is passing through the coil. If this waveform is correct, suspect the YIG oscillator. Refer to the RF Section Service Sheet.

3. Check TP16. This voltage should track the YO DRIVE V (Figure 8-46). If it does not, troubleshoot U24, Q1, Q2, A9R1, and A9Q1.

   a. To verify proper operation of U24, ground TP16 (R1 is a 12 Watt resistor). Press 8350A CW . Vary the voltage at U24 pin 3 by changing the CW frequency as indicated on the front panel. With TP16 at 0 Vdc, U24 pin 6 should be at approximately +20 Vdc for positive input voltages, and approximately −10 Vdc for negative input voltages. If it is not, replace U24.

   b. A9R1 should be checked by removing the A9 assembly from the instrument. The ohmmeter reading should be approximately 125 ohms.

   c. While the A9 assembly is removed from the instrument, check the collector-base and base-emitter junctions of A9Q1 with an ohmmeter. These junctions should show only a few hundred ohms when forward biased, and a high impedance in the reverse direction. If A9Q1 is found to be shorted or opened, make sure that protection diodes VR1 and CR6 are good before replacing the transistor.

   d. Q1 and Q2 can be checked, using the procedure above, while they are still in the circuit. The line power should be off.

Interrupt Control

Symptoms of an interrupt failure may include loss of sweep, portions of the sweep trace missing, or a false bandswitch.

1. Place the A6 assembly on an extender board. With an oscilloscope, check P1-23 (L SSRQ) for approximately +4.5 Volts. Since the band-switch circuitry is disabled, the only time L SSRQ should be low is when used in conjunction with external equipment requiring a stop sweep, or when programmed through the 8350A auxiliary programming connector.

   a. If L RTS is low, check that U5 pin 3 is at 0 Volts. If it is not, check the L BSE line for approximately +4.5 Volts. Then troubleshoot U26.

   b. If U26 is good, ensure that U17A pin 5 is not held high. If it is good, other lines are probably pulling L SSRQ low. Refer to the 8350A Operating and Service Manual for more troubleshooting information to determine the problem.

2. Check edge connector pins P1-3 (LSIRQ) and P1-1 (L RTS).

   a. L RTS should appear as illustrated in Figure 8-50 with a low pulse occuring at the end of each forward sweep. If L RTS is not correct, trace the problem back through the plug-in interconnects to the 8350A.

   b. LSIRQ should pulse low briefly for end-of-sweep interrupts as illustrated in Figure 8-50. If these pulses are missing, but L RTS is present, suspect U21C, U17B, or control lines from U22.

   c. If L SIRQ stays low, or the pulses are exceptionally wide, check U22 with the procedure outlined under **Digital Control** section. If U22 is functioning, the 8350A microprocessor probably did not receive the interrupt. Trace this signal back to the 8350A.

Digital Control

The Address Decoder, Input Data Latches, and Frequency Cal Switches/Output Data Buffers comprise the digital control for the A6 assembly. A failure in these components usually results in large frequency errors, and will often disable the bandswitch circuitry.

To check the address decoding circuitry enter **SHIFT** 5 4 and perform the following:

1. Examine LINST2 (P1-18) for activity. If none is found, troubleshoot the A3 assembly.

2. If LINST2 is functional, check each of the LENn lines (U25) for the pulses shown in Figure 8-52. If these are incorrect, but the address lines show activity, replace U25. If the address lines seem locked high or low, troubleshoot the address buffer on the A3 assembly.

NOTE

U3, U4, and U7 are checked by reading data while changing switch settings. Before altering the switch settings on A6S1 and A6S2, note the present configuration. Return the switches to their original status after troubleshooting. If this is not done, the frequency endpoints will have to be recalibrated.

3. To check status buffer U7, press **INSTR PRESET** . Set the 8350A for a 5-second sweep rate and make the following key entries:

SHIFT 0 0	Enters the Hex Data command
2 GHz s 8 6	Address location 2C86 (U7)
M3	Hex Data Read

The hex digits displayed in the 8350A front panel FREQUENCY/TIME window should change as the status read by U7 changes between forward sweep and retrace. Raising the power level until the UNLEVELED light comes on should also change the status bit being read by U7. Switches S1 and S2 can be toggled to test the two last bits.

4. U3 and U4 can each be checked with Hex Data Read (see above) at address 2C84 or 2C85. The hex digits should change when the corresponding Freq Cal switches are changed.

5. Exercise U22 with Hex Data Rotation Write. Enter:

SHIFT 0 0	Enters Hex Data command
2 GHz s 8 3	Address location 2C83 (U22)
M4	Hex Data Rotation Write

Check the outputs of U22 against the waveforms shown in Figure 8-2.

6. The remaining three latches-U8, U13, and U18-can be checked by selecting a CW frequency of 2.4 GHz and pressing **SHIFT** 5 2 . to initiate the Scaling/Offset DAC Test. The waveforms at TP1 and TP2 should be checked against those in Figure 8-53.

a. If these are faulty, check the outputs of the latches, and replace them if necessary. If the bit patterns are correct, but the waveforms are not, replace the appropriate DAC.

−10V REF

Check TP3 for −10 Vdc ±1 mV. If this voltage is incorrect, perform the −10V Reference adjustment procedure provided in Section V of this manual. If the adjustment cannot be made, check U23 pin 2 for −6.95 Vdc ±0.15 mV. If this voltage is incorrect, replace U23. Check U20 pins 2 and 3 for −6.95 Vdc ±0.15 mV. If either measurement is incorrect, troubleshoot U20 and associated circuitry.

5V Regulator

Check A9Q3 pin 1 for slightly over +5 Vdc, and trace the line back to the 8350A if the voltage is missing. Remove A7, A8, and RF ribbon cable W16 to check for the possibility of excess loading. Then check A9Q3 pin 2 for +5 Vdc. If incorrect, replace A9Q3.

CW Filter

Relay K1 and C14 reduce residual FM by filtering the noise from the YO Coil current. The relay is actuated by a line from U22. To check the data line, press 8350A CW . Enter:

SHIFT 0 0	Enters Hex Data command
2 **GHz s** 8 3	Address location 2C83 (U22)
M2	Hex Data Write
0 0 / **BKSP** **BKSP**	Enters hex data 00 and FF

Alternate between 00 and FF. Check U22, pin 6. If it is dead, make sure protection diode CR5 is good. Then replace U22.

If U22 is working, alternate between 00 and FF, as described above, and verify that contacts in relay K1 are opening and closing.

A9P1

PIN	SIGNAL	I/O	TO/FROM	BLOCK
1 7	BASE +5V REG	IN OUT	A6P1-22 A9P1-7	M L
2 8	COLLECTOR NC	OUT	A6P1-41	M
3 9	+20V NC	IN	P1-7	M
4 10	EMITTER/COIL NC	OUT	A6P1-20	M
5 11	+20V FREQ REF +20V	OUT IN	A6P1-21 P1-7	M M
6 12	GND ANLG +5V UNREG	IN	P2-27,58,59 P2-62,63	L L

A9

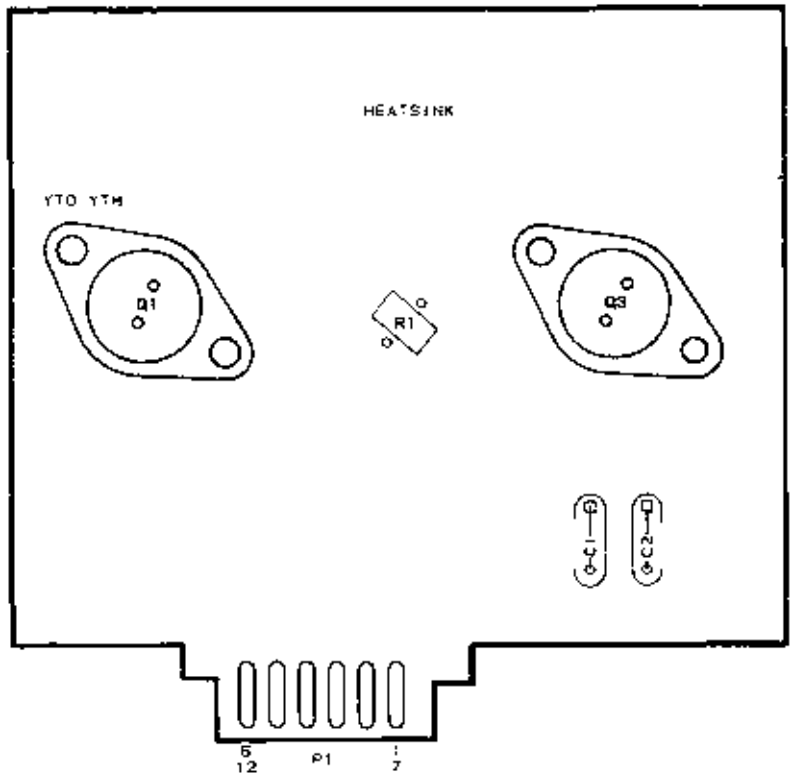


Figure 8-44. A9 Reference Resistor, Component Locations

Figure 8-48. Delay Compensation (A6TP6)

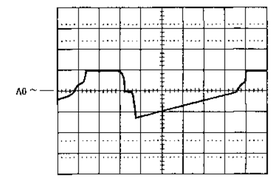


Figure 8-47. YO DRIVE Voltage (A6TP14)

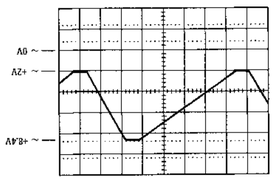


Figure 8-46. Emitter/Coil Voltage (A6TP12)

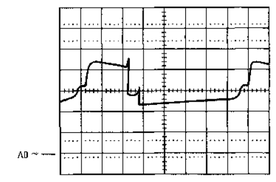
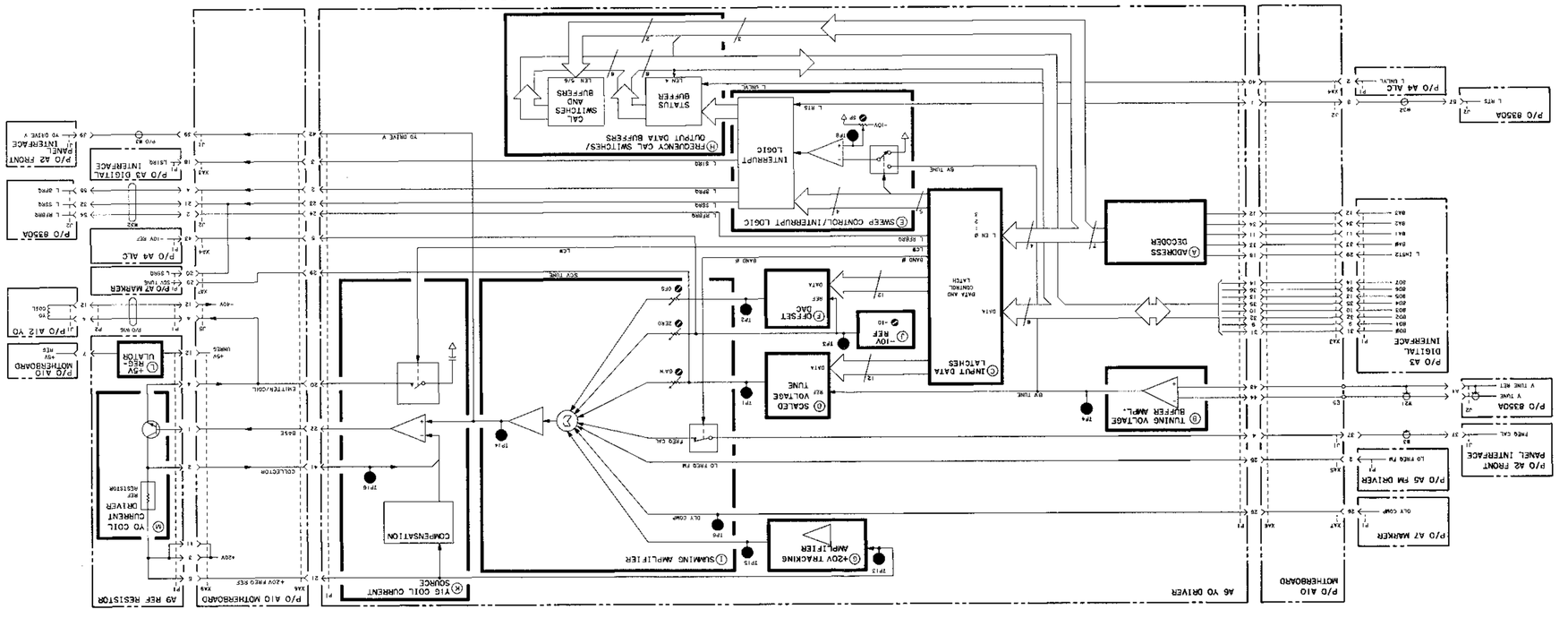


Figure 8-45. A6 YO Driver, Block Diagram



A7 MARKER ASSEMBLY, CIRCUIT DESCRIPTION

The A7 Marker and A8 Sampler Assemblies combine to provide crystal referenced frequency markers at 10 MHz or 50 MHz intervals over the frequency range of 0.01 to 2.4 GHz and 1 MHz intervals in the 0.01 to 1 GHz range in the 83522A.

In addition to the internal crystal referenced markers, markers may be generated whenever the sweep oscillator output frequency is the same as that of an external signal source applied to the External Marker input on the plug-in rear panel. This feature is useful for obtaining markers which are not an integral multiple of 1, 10, or 50 MHz.

Two types of markers are available. Intensity markers of a CRT trace are available through the intensity modulation outputs on the rear panel of the 8350A Sweep Oscillator. Amplitude markers of approximately 1 dB are available on the plug-in RF Output. In addition, when either intensity or amplitude markers are selected, an LED marker indicator on the plug-in front panel is turned on by any marker occurrence.

Marker mode as well as marker frequency is selectable by either a front panel pushbutton or through HP-IB control.

The A7 Marker assembly also provides the following functions:

- The RF Switch Driver controls PIN diode RF switches in multiband plug-ins. This circuit is not used in the 83522A.
- The Oscillator Bias Shaping Control shapes and controls the negative bias signal to the A12 YIG Oscillator. A high (0V) on L RFON (L=RF ON) turns off the A12 YIG Oscillator as controlled by the front panel RF ON/OFF pushbutton.
- The Delay Compensation circuits compensate the A12 YIG Oscillator for swept frequency inaccuracy caused by delay in the oscillator tuning coil at fast sweep times.

Marker Circuits.

The A7 Marker circuits accept the BIRDIE signal from the A8 Sampler. This BIRDIE signal consists of a square wave beat frequency which is the result of a portion of the RF Output signal being mixed with an internal comb or external marker reference frequency. The beat frequency is converted to a square wave by the A8 Sampler Squarer circuit so that the fast rising edge of the BIRDIE signal can accurately trigger the marker timer circuits on the A7 Marker board. The marker circuits include a programmable pulse width discriminator which compares the time period of the input BIRDIE pulses to a minimum time period reference. This reference time period is varied by the Marker Threshold circuit depending upon which front panel MARKER FREQUENCY is selected. If the time period of the BIRDIE pulses is greater than the reference time period, a valid marker will be output. Markers will be disabled by the Pulse Modulation Logic whenever the RF Output is turned off, such as when RF modulation is used. If Intensity Markers are selected, L ZMKR (L=INTENSITY MARKER REQUEST) is sent to the 8350A Sweep Oscillator to be processed for the POS Z BLANK and NEG Z BLANK rear panel BNC outputs. If Amplitude Markers are selected, L DBMKR (L=1 dB MARKER MARKER REQUEST) will signal the A4 ALC board to modify the power level of the RF Output to cause a dip of approximately 1 dB at the marker occurrence.

Address Decoder (A)

The A7 Marker and A8 Sampler use address locations 2C01H, 2C02H, and 2C03H. U14 is a 3-to-8 address decoder which produces 3 active low control signals when an address associated with the Sampler or Marker assemblies is present on the plug-in address bus. These signals are used to latch control information from the data bus into latches U9 and U13 on the Marker assembly and into U10 on the A8 Sampler.

Marker/RF Switch Control (B)

When L EN3 goes low, control information from the data bus is latched through U9 to control the Marker Threshhold adjustment circuits and marker type. The RF switches are not installed in the 83522A, therefore, the switch control lines are not used.

Marker On (E)

The incoming BIRDIE signal from the A8 Sampler Squarer circuit is inverted by U4D and then applied to the ON interval comparator U1B and delay network R1, C1. When the input BIRDIE pulse train goes from high to low at TP3, it causes U1B to trigger and U1A pin 1 to go high. Delay network R1, C1 keeps the signal at U1A pin 2 from going high until the signal on U1A pin 1 goes high, allowing for the propagation delay in U1B. This condition is sustained until either the input signal goes high again causing U1A pin 2 to go low or timer U1B times out causing U1A pin 1 to go low. In the first condition, nothing happens. In the second condition, U1A triggers causing U1A pin 4 to go low resulting in a marker being generated and the front panel marker LED being turned on. Therefore, the Marker On timer U1A outputs a pulse whenever the BIRDIE pulse periods are longer than the reference time period set by U1B.

The type of marker generated depends on the digital control lines AMKR (H=Amplitude Marker) and ZMKR (H=Intensity Marker) enabling U4B and U5D, respectively. A high signal on U4B pin 4 (AMKR) enables U4B pin 6 to go low driving inverter U12A pin 1 high. This causes U2B pin 7 to go low and signals the A4 ALC board to generate an amplitude marker. Similarly, a high on U5D pin 12 (ZMKR) enables U5D and causes an intensity marker to be generated by the 8350A Sweep Oscillator. Markers may be prevented from occurring by a low signal on the clear input of U1A pin 3. Whenever a valid marker is generated, U1A pin 4 pulls L MKRLED (L=Marker LED on) low and the front panel MKR LED is turned on once for each marker occurrence.

U15A is a marker stretcher circuit. If the sweep oscillator RF output is shut off by a low L PULSE signal from the Pulse Modulation Logic during the time in which a marker is being generated, U15A triggers and causes the marker to continue, even when U1A pin 3 has gone low and driven the Marker On output at U1A pin 4 low. This stretching of several microseconds keeps the marker signal from being shut off prematurely by short modulation pulses such as those encountered when the 8350A is used in conjunction with an 8755C Swept Amplitude Analyzer. The sweep speed may be slowed when modulation is used to improve marker consistency and avoid "beating" between marker and modulation pulses.

Marker Threshold (C)

The Marker Threshold is adjusted by R7, R6 and R5 which are selected by U2D, U2C, and U2A via the digital control lines for 1, 10, and 50 MHz marker frequencies, respectively. R5 also adjusts the marker threshold when external markers are selected. These adjustments vary the charging current for the timing capacitors in marker timers U1B and U8A simultaneously, thus varying the reference pulse width out of U1B and U8A.

Marker Off (F)

The Marker Off circuit turns off a previously generated Marker On signal when the BIRDIE low period is shorter than the reference time period pulses or when the sweep oscillator RF output has been turned off by the Pulse Modulation Logic circuit. The Marker On pulse width could otherwise cause a marker to be output after the sweep oscillator frequency has swept above the comb frequency or the external input frequency. U8A serves as the threshold detector by firing whenever the BIRDIE input goes low. This low signal is also applied to U8B pin 9 and enables U8B. When U8A pin 13 triggers, it causes U8B pin 10 to go high. If the BIRDIE signal does not return high before U8A times out, no output is generated by U8B. This would happen if the BIRDIE low period is longer than the reference time period. If the BIRDIE signal returns high sooner than the reference time period of U8A, this allows U8B pin 10 to return low, and a Marker Off pulse is generated at U8B pin 5. Either this signal or the L PULSE signal causes U12C pin 10 to go low and turns off the marker timer U1A.

Pulse Modulation Logic (D)

The Pulse Modulation Logic circuit provides the L PULSE output that is primarily used to amplitude modulate the RF output. When L PULSE is low, the RF Output is effectively turned off. The actual modulation drive current is provided by the A4 ALC Assembly. The L PULSE output is also provided to the Marker On circuit where it is used to control a marker stretcher circuit. The Pulse Modulation Logic circuit provides a low L PULSE signal if any one of the RF Marker (L RFM), Internal Squarewave Modulation (SQ MOD), or External Squarewave Modulation (PULSE IN) signals are present. The resistor diode network on U5C pin 10 translates the (PULSE IN) 8755 Modulation Drive to TTL levels but does not affect TTL inputs.

Delay Compensation Control (G)

U13 latches the Delay Compensation control lines to the appropriate circuits as controlled by the L EN1 line from Address Decoder U14. Buffered data lines BD1 through BD6 are used as the control inputs to the various delay compensation circuits.

Delay Compensation (I)

The delay compensation block circuitry is used to compensate the A12 YIG Oscillator for the inherent inaccuracy caused by delay in the magnets at fast sweeps. The input signal is SC VTUNE, a scaled ramp from the A6 YO Driver, the slope of which is proportional to the change in frequency. SC VTUNE is sent to two separate signal processors: 1) a Voltage Follower/Subtractor whose output is equal to zero at start of sweep and at the band switch point. The amplitude is proportional to sweep width, and 2) a Differentiator whose output is proportional to the rate of frequency change while sweeping. These two signals are then multiplied in the Analog Multiplier U7. The multiplier signal is summed with the bandswitch compensation (corrects for errors at bandswitching points) in multi-band plug-ins. This bandswitch compensation signal is not enabled in the 83522A. If the sweep oscillator is in a swept mode, U11A enables the delay compensation which is summed into the main coil driver voltage on the A6 YO Driver.

During retrace, analog switch U11B closes. In this condition, U10 together with R39, R41, R42, and R43 form a subtractor circuit. Both inputs are the input signal so they cancel in the operational amplifier and the resulting output is 0V, regardless of the input level. With U11B closed, C17 charges to one half the value of the input signal (R41 and R42 form a voltage divider) U11B opens again during the sweep which leaves only C17 in the feedback path of U10. Since there is no discharge path with U11B and U11C open, C17 remains charged to the 1 just before U11B was opened. U10 now operates as a voltage follower, with the output level shifted by the voltage across C17. Therefore, the output of U10 has one half the slope of the input signal and returns to 0V whenever U11B is closed during retrace. The output of U10 is scaled by the HI adjust potentiometer and is applied, with an offset from the LO adjust potentiometer, to inverting amplifier U3B. The output generated at TP5 is one input to the analog multiplier.

If the sweep is stopped momentarily, such as when an external counter is used, L SSRQ is pulled low by the 8350A mainframe. L SLSMPL enables gate U5A and allows the L SSRQ line to control analog switch U11C. When U5A is enabled by a low on the L SLSMPL control line, and L SSRQ goes low, U11C closes and slowly recharges C17 through R40. Thus, when L SSRQ is pulled, the output of U10 will begin to go to zero volts, but may or may not reach zero volts depending on the length of time L SSRQ was pulled. This is done when in CF ΔF mode where ΔF equals zero. When L SSRQ goes high again and the sweep continues, U11C opens and U10 resumes its voltage follower operation.

SC VTUNE is also applied to Differentiator C15 and U3D. The output is amplified and inverted by U3C and is applied at TP4 to the second input of the analog multiplier. The output at TP6 is connected to U7 pin 7 to provide feedback for an operational amplifier internal to U7. The Z adjust at U7 pin 6 allows nulling of the offset voltage appearing at DLY COMP. This is done when in CF ΔF mode where ΔF equals zero. The YIG Oscillator does not always naturally settle to the proper start frequency after retracing. For fast, repetitive sweeps, the frequency during the first part of the band will be higher than it should be, unless it is corrected. CR9, C22, R63, and R64 correct for this condition by charging C22 to the output voltage of the differentiator during retrace and then allowing it to discharge through R63 and R64 into summing amplifier U3A. Q3 disables this function during sequential or alternate sweeps by shunting R63 and R64 to ground.

U11D is momentarily closed during bandswitching in multi-band plug-ins. It is held open at all times in the 83522A.

The output of U3A is then sent to the A6 YO Driver where it is summed into the main coil driver voltage. Since the delay compensation is unnecessary during CW operation, annlog switch U11A disables DLY COMP output to ground.

RF Switch Driver (H)

The RF switches are not intalled in the 83522A and, therefore, the switch driver circuits are not used.

Oscillator Bias Shaping Control (J)

U6A, U6B, and Q1 shape and control the negative bias signal to the A12 YIG oscillator. A frequency related YO DRIVE Voltage is applied to U6B. By adjusting the network of variable resistors R20, R21, R26, and R27, the YIG Oscillator bias can be controlled for optimum operation. A high state on the L RFON line allows the oscillator bias to be removed when it is desired to turn off the oscillator. Q1 serves as a high current output stage to provide adequate bias current for the YIG Oscillator.

Table 8-11. Marker Assembly Address Decoding

Address (Hexadecimal)	Components Addressed	Read or Write	Description
2C01	A7U13	Write	Addresses data latch to provide Delay Compensation control.
2C02	A8U10	Write	Addresses data latch on the A8 Sampler to provide digital control.
2C03	A7U9	Write	Addresses data latch for Marker/RF Switch control.

A7 MARKER ASSEMBLY, TROUBLESHOOTING

Component failures on the A7 Marker Assembly may be classified as either Digital Control, Marker, Delay Compensation, Oscillator Bias, or Pulse Modulation Logic failures. Digital circuitry in blocks A and B control the Markers and Delay Compensation circuits. Failures in these circuits may cause failure symptoms in the various functions performed by the A7 assembly. Therefore, the troubleshooting guide verifies these blocks first.

Digital Control

All data bus and control lines may be effectively checked by making use of the Hex Data programming and Operator Initiated checks available through software.

To verify Address Decoder U14, press 8350A CW . Then enter SHIFT 5 4. In this mode, the 8350A microprocessor continuously strobes the plug-in

A6

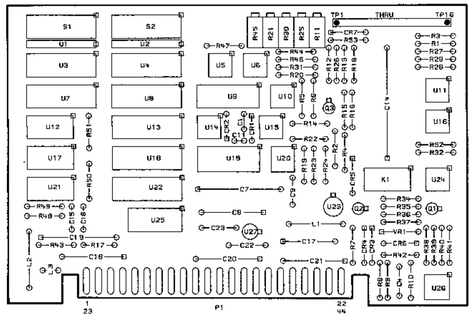


Figure 8-49. A6 YO Driver, Component Locations

A6P1

PIN	SIGNAL	I/O	TO/FROM	BLOCK
1 23	L BTS L SSRQ	IN	P2-57 NOT USED	E H
2 24	L BPRQ L RFBRQ		NOT USED NOT USED	
3 25	L SIRQ LO FREQ FM	OUT IN	A3P1-18 A5P1-2	E I
4 26	FREQ CAL OLY COMP	IN IN	A10J1-37 A7P1-26	I I
5 27	−10V REF +5V	OUT IN	A4P1-43 A3P1-6,7	J L
6 28	−40V −15V	IN IN	P1-11 P2-28	L L
7 29	+10V SCVTUNE	IN OUT	P1-8 A7P1-29	L D
8 30	GND DIG GND DIG			L L
9 31	BD1 BD0	I/O I/O	A3P1-9 A3P1-31	CH CH
10 32	BD3 BD2	I/O I/O	A3P1-10 A3P1-32	CH CH
11 33	BA1 BA0	IN IN	A3P1-11 A3P1-33	A A
12 34	BA3 BA2	IN IN	A3P1-12 A3P1-34	A A
13 35	BD5 BD4	I/O I/O	A3P1-13 A3P1-35	CH CH
14 36	BD7 BD6	I/O I/O	A3P1-14 A3P1-36	CH CH
15 37	PWON GND ANLG	IN	P2-25	C L
16 38	+20V +15V	IN IN	P1-7 P2-29	L L
17 39	−10V −40V	IN IN	P1-13 P1-11	L L
18 40	L INST2 L UNLVL	IN IN	A3P1-29 A6P1-2	A H
19 41	GND ANLG COLLECTOR		A9P1-2	L K
20 42	EMITTER/COIL YO DRIVE V	OUT	A9P1-4 A7P1-5 A10J1-39	K I
21 43	+20V FREQ REF VTUNE RET	IN OUT	A9P1-5 P1-A1	K B
22 44	BASE VTUNE	OUT IN	A9P1-1 P1-A1	K B

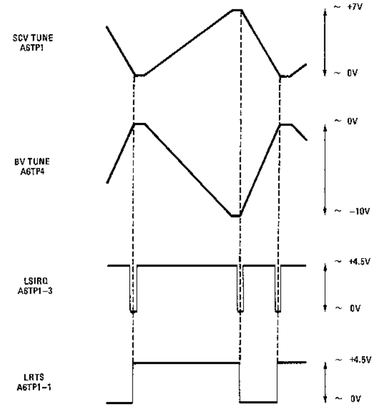
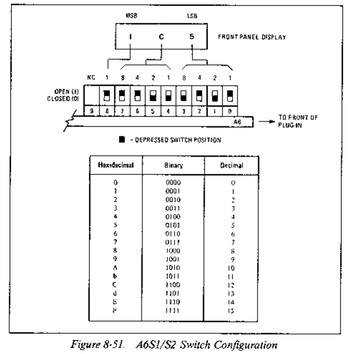


Figure 8-50. Sweep Control and Interrupt Logic Waveforms



Hexdecimal	Binary	Decimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
A	1010	10
B	1011	11
C	1100	12
D	1101	13
E	1110	14
F	1111	15

Figure 8-51. A6S1/S2 Switch Configuration

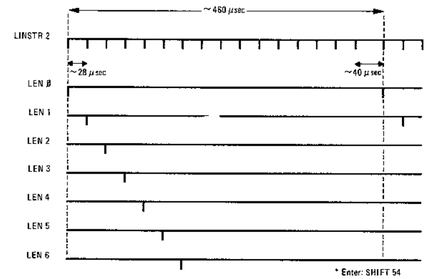
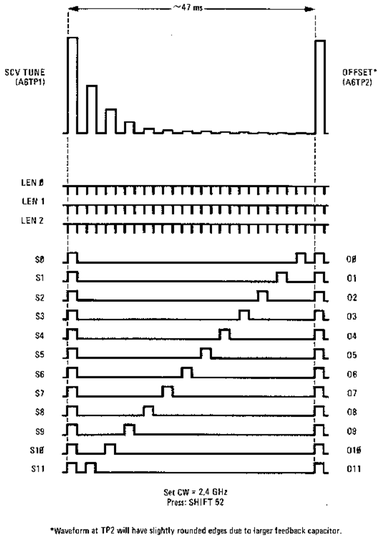


*Figure 8-52. A6 Decoder Timing Diagrams**



*Waveform at TP2 will have slightly rounded edges due to larger feedback capacitor.

Figure 8-53. DAC Test

NOTES

1. THE FOLLOWING KEY ENTRIES PROVIDE FRONT PANEL ACCESS FOR A DATA WRITE/READ OPERATION TO/FROM THE ADDRESSED LOCATION:

FUNCTION	KEY ENTRY
*Hex Address Entry	SHIFT 0 0 (enter hex address)
Hex Data WRITE	M2 (enter data: two hex digits)
Hex Data READ	M3
Hex Data Rotation Write	M4
Hex Addressed Fast Read	M5

*TO ADDRESS A DIFFERENT LOCATION, PRESS M1 AND ENTER THE NEW ADDRESS, OR USE THE INCREMENT KEYS ▲ ▼ TO STEP TO THE NEW ADDRESS.

TO PREVENT THE MICROPROCESSOR FROM SERVICING THE RETRACE INTERRUPT, PRESS 8350A CW .

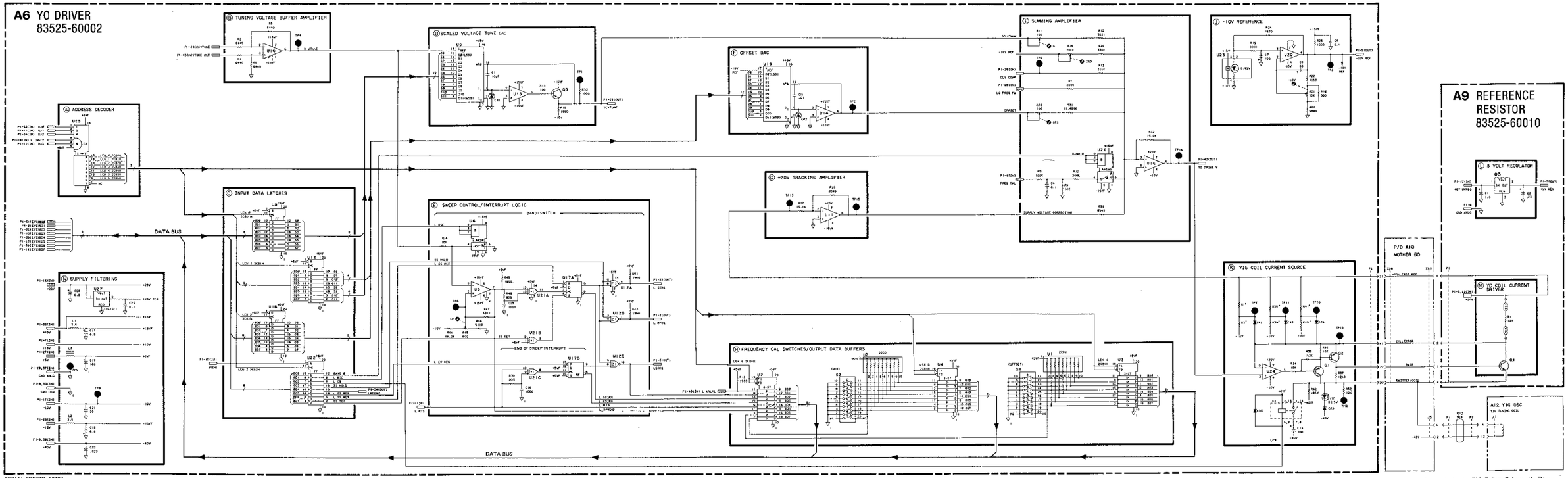


Figure 8-54. A6 YO Driver Schematic Diagram

Verify operation of U9. Marker/RF Switch Control, by making the following key entry:

Press 8350A INSTR PRESET CW

SHIFT 0 0	Hex Data mode
2 GHz s 0 3	Address location 2C03 (U9)
M2	Hex Data Write
5 5	Enters byte with alternate high/low states

Check the outputs of U9 for the alternating high/low pattern. To obtain the complement of each of the U9 outputs, press . . (AA). This will expose any locked latch registers.

To verify operation of U13. Delay Compensation Control, make the following key entries:

M1 2 GHz s 0 1	Address location 2C01 (U13)
M2	Hex Data Write
5 5	Enters byte with alternate high/low states

Check the outputs of U13 for the alternating high/low pattern. To obtain the complements of each of the U13 outputs, press . . . Check the outputs of U13 again.

Markers

To troubleshoot A7 for marker failure symptoms, start by using an oscilloscope to check Test Points 1, 2, and 3.

Press 8350A:

INSTR PRESET
CF 1 GHz s
ΔF 1 MHz ms
TIME 1 0 MHz ms

Press 83522A:

AMPTD MRK

Engage the 1 MHz frequency marker and check TP1. The signal should represent a TTL pulse approximately 2 cm wide. See Figure 8-57. Likewise, the pulse at TP1 should be 4 cm wide for 10 MHz Markers, and 6 cm wide for 50 MHz Markers. If these pulses appear to be incorrect, check that analog switch U2A,C,D is switching properly. If it is, check the output pulse widths of the monostable multivibrators against the data given in Table 8-12.

Check TP3 for the Birdie signal illustrated in Figure 8-57. (The birdie can be centered on the screen with the front panel **FREQ CAL** knob.) If the waveform is incorrect, refer to A8 troubleshooting.

Check TP2 for the waveform shown in Figure 8-57. These Marker OFF pulses should surround the Marker ON pulses at TP1. If these are incorrect, check the outputs of the monostable multivibrators against the data in Table 8-12.

Table 8-12. Approximate Monostable Multivibrator Pulse Times

U1B	8 to 10 μsec
U8A	1 to 10 μsec
U8B	75 nsec
U15A	88 μsec

Delay Compensation

Before troubleshooting the A7 assembly for delay compensation failures, refer to the A6 Service Sheet and verify the YO Drive Voltage at A6TP14. If this signal is correct, begin troubleshooting the A7 assembly by checking the waveforms at TP 4, 5, and 6. Press 8350A **INSTR PRESET** .

Test point 4 shows the compensation for the abrupt change in tuning current at the start of a sweep (Figure 8-58). The amplitude of this signal decreases as sweep time increases. Test point 5 shows the compensation for current lag in the YO with respect to sweep voltage (8-58). Test point 6 shows the sum of TP 4 and 5 signals (Figure 8-58). These checks should isolate the problem to one of the following circuits: Voltage Follower Subtractor, Differentiator, Analog Multiplier, or Delay Compensation Enable/Bandswitch Compensation.

Oscillator Bias Shaping Control

Check TP7 with a voltmeter while switching the plug-in RF power switch on and off. With the RF on, TP7 should be approximately −9.8 Vdc. With the RF off, TP7 should be approximately 0 Vdc.

Pulse Modulation Logic

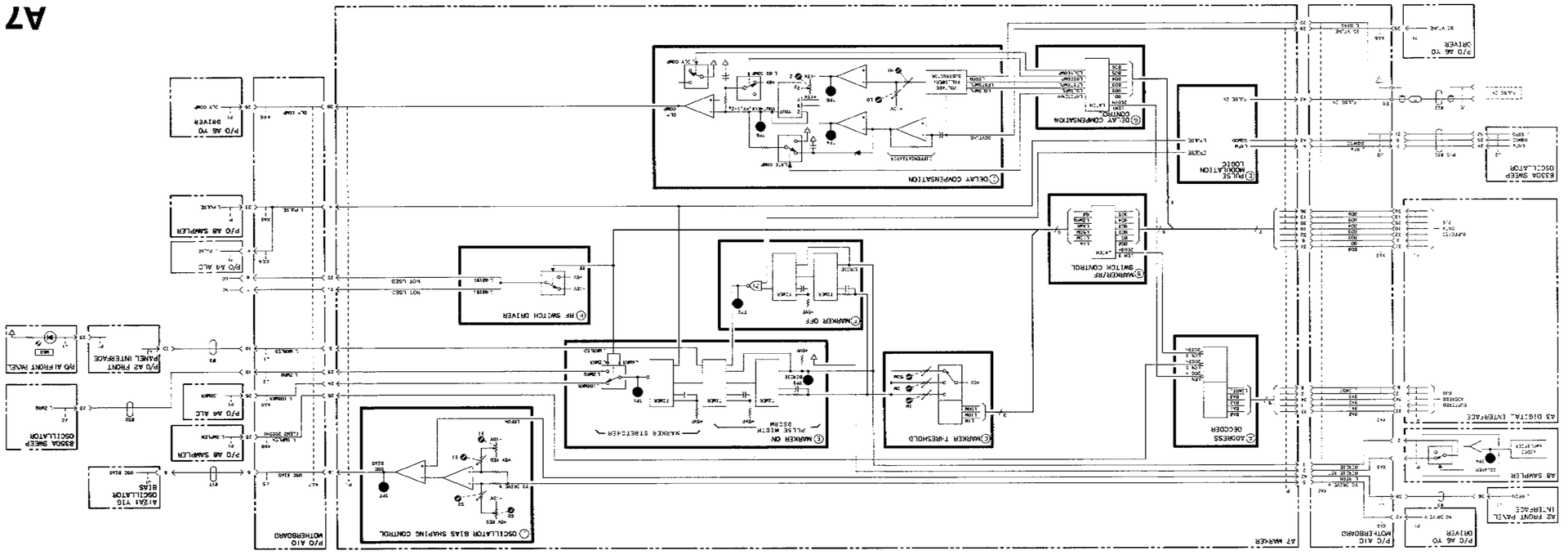
Enable 8350A ⌐¬ **MOD** and check pin 13 of U12D for the proper square wave signal: 27.8 or 1 kHz.

RF Switchdriver

RF switches are not installed in the 83522A and, therefore, the switch driver circuits are not used.

A7

Figure 8-55. A7 Marker, Block Diagram



A8 SAMPLER, CIRCUIT DESCRIPTION

The A8 Sampler accepts an RF signal from the DCI Directional Coupler/Detector AUXiliary output port which is mixed in one of two mixers with the rear panel EXT MKR input or the comb generator output signal. The comb generator output consists of a selected 1 MHz, 10 MHz, or 50 MHz frequency multiples source. The mixer used supresses all output signals except the lower sideband which is then used as a birdie signal. The birdie is then sent to the programmable low pass filter to ensure that only the lowest frequency birdie is used. This birdie is then the result of a single Comb Generator harmonic which is closest in frequency to the input RF signal. The birdie is amplified in the variable gain video amplifier so that a constant level, regardless of input RF frequency and power level, can be sent to the Squarer. The Squarer converts the birdie signal to a TTL level compatible signal which is then used to generate a marker on the A7 Marker board.

Digital Control (A)

The L SMPL EN input from the Address Decoder on the A7 Marker assembly clocks data into data latch U10. These latched data lines provide digital control of the sampler board. Resistor array U12 provides pullups to ensure that the high level on the control lines is near +5V.

50 MHz Oscillator (C)

The frequency determining network of the 50 MHz Oscillator is formed by crystal Y1, resonant tank circuit C1 and L1, and capacitors C3 and C4. C4 is used to fine tune the center frequency of the oscillator to 50 MHz. Resistor R1 is used in conjunction with L1 and C1 to ensure oscillations at 50 MHz. U11B provides a buffer stage for the oscillator. R3 and R4 provide the necessary pulldown for the outputs of ECL devices U11A and U11B.

Frequency Divider Circuits (F)

Integrated circuits U6 and U9 are ECL bi-quinary dividers, having both divide-by-two and divide-by-five circuits built in. The output of the 50 MHz Oscillator is applied at the input of the divide-by-five portion of U9. When U9 is selected by a low on the digital control line through CR3, it produces one-fifth of the input frequency, or 10 MHz at U9 pin 4. This 10 MHz signal is applied simultaneously to the divide-by-five input of U6 and to the gate U7B. Both divider circuits are used in U6. The output of the divide-by-five is fed back to the input of the divide-by-two, resulting in a divide-by-ten circuit. The result is an output of 1 MHz at U6 pin 15 when both U6 and U9 are enabled by lows on their respective control lines. Selection of the desired frequency is done through the use of the digital control lines on the divider circuits U6 and U9 as well as gates U7A, U7B, and U7C.

For 50 MHz markers, U9 and U6 are disabled by a logic high on their reset inputs (pin 9), and the 50 MHz Oscillator output is gated through NOR gates U7A and U7C.

For 10 MHz markers, U6 is disabled, and the 10 MHz output from U9 is gated through U7B and U7C; the U7A output is kept low by a logic high on the L 50 MHz logic line.

For 1 MHz markers, the 1 MHz output from U6 is gated through U7C and the U7A and U7B outputs are kept low by logic highs on their inputs.

Resistors R6, R8, R11, R12, and R27 provide the necessary pulldown for the outputs of the ECL logic. Diodes CR2 and CR5 in the digital control lines and resistors R5, R7, R9, and R10 provide the necessary interface between the TTL digital control and the ECL logic.

Comb Generator (H)

The 1, 10, or 50 MHz square wave at TP2 is applied to the inverting and non-inverting inputs of U11C and U11D, respectively. This causes the differential voltage across the Comb Generator diode CR8 to be twice the normal ECL logic voltage swing or about 1.6V. The output of CR8 is coupled through C14 to the Internal Mixer diode CR7. This output signal is a spectrum of frequencies at multiples of the input frequency to the comb generator (1, 10, or 50 MHz).

U11C pin 9 provides an input bias level for all parts of U11. This bias is applied through R64 on the Comb Generator and R2 on the 50 MHz Oscillator.

RF Power Divider (B)

The RF Power Divider divides and shapes a portion of the sweeper output signal and sends it to the Internal and External Mixer circuits. The signal input at J1 may range from about −25 dBm to about −10 dBm. The output signal to the two mixers will be slightly below this level, depending upon input frequency.

Internal Mixer (E)

Internal Mixer Diode CR7 mixes a portion of the sweeper output signal with the frequency comb produced by the comb generator circuit. The circuit including Q2A and Q2B produces an output of only the difference frequency of the two inputs. The sum frequency is attenuated by the circuit's high impedence and parasitic capacitances. Therefore, as the sweep oscillator output frequency approaches that of one of the Comb Generator harmonics, a difference frequency appears at the internal mixer output through R28. This frequency decreases to zero Hz when the sweep oscillator output frequency is identical to that of the Comb Generator harmonic and then increases in frequency as the sweep oscillator output frequency moves higher. The resulting waveform is referred to as a birdie. Bias for CR7 is provided by the constant current stage Q5. The Q5 current output is adjusted by R29, R30, and R31 for 1, 10, and 50 MHz marker frequencies respectively.

External Mixer (D)

The External Mixer operates in a similar manner as the Internal Mixer with the exception that it uses an externally provided signal rather than the Comb Generator signal. A similar output birdie is obtained. CR6 mixer diode bias is maintained by R17. Q4A and Q4B provide a high impedence follower identical to Q2A and Q2B. The External Mixer is selected by applying 0V at the gate of FET switch Q3. The internal 50 MHz crystal oscillator and the Frequency Divider Circuits are disabled when the external marker mode is selected.

Programmable Low Pass Filter (G)

Birdies from either the Internal and External Mixers are applied to emitter follower Q1. This stage provides a low impedance source for the Low Pass Filter circuits. Multiplexer U4B selects one of the following filters: approximately 300 kHz LPF, approximately 4 MHz LPF, or the filter bypass line. The Low Pass Filters insure that the birdie is a result of only one comb frequency at a time.

Video Amplifier (J)

U3 and U1 amplify the birdie signal from the output of the Low Pass Filter from a level of a few millivolts to a level of about one volt. Because the level of the incoming birdie signal can change as a function of the marker frequency and the RF OUTPUT level, a means to control the gain of the video amplifier is necessary. This is accomplished by varying the bias current into U3 pin 7 and U1 pin 7. The bias current for U3 pin 7 adjusts the gain to compensate for instrument RF OUTPUT power level changes. The bias current into U1 pin 7 adjusts the gain to compensate for variations in the amplitude of the birdie signal when different marker frequencies are selected. This current is adjusted by R53, R54, R55, and R67 when 1 MHz, 10 MHZ, 50 MHz, and EXTernal marker frequencies are selected, respectively. Multiplexer U5 selects the appropriate adjustment as well as switching in an additional shaping capacitor when 1 MHz markers are selected. This capacitor helps to further low pass filter the 1 MHz birdie signal. U5 also provides control lines to select the proper bias for the internal mixing diode CR7 and to select the External Mixer when required.

Gain Shaping (I)

The Gain Shaping circuit alters the gain of Video Amplifier U3 so that as the sweep oscillator RF output level changes, the amplitude of the birdie signal remains relatively constant. The power reference signal from the ALC board is amplified in U8A and is applied to U8B along with an offset voltage from R65. With low power output, the power reference voltage is only slightly negative. At this level, CR11 clamps the voltage at the output of U8B to about +0.6V. As the RF OUTPUT power level is increased, this voltage decreases and causes the current into U3 pin 7 to decrease, reducing the Video Amplifier gain. This keeps the amplitude of the birdie signal at TP4 relatively constant regardless of RF power output variations.

Squarer (K)

The Squarer circuit provides TTL compatible signals for the rest of the marker circuits located on the A7 Marker assembly. U2 is a voltage comparator which compares the incoming birdie to an approximately −0.1V reference established by resistor divider R58 and R59. Resistor R60 provides some hysteresis for the stage. The effect of these resistors is to improve the noise immunity of the circuit. U4A is an analog switch which provides drive for the TTL circuitry and serves as a transition point for the two different ground returns on the A7 and A8 boards. This is important because the high gain on the A8 Sampler assembly would be particularly susceptable to pick-up from the fast rise time digital signals on the A7 Marker assembly.

The Squarer circuit can be disabled either by a low signal on the digital control line to U2 pin 6 or by a low signal on the LPULSE line to U2 pin 5. The LPULSE line disables the Squarer output any time the sweep oscillator RF output is absent due to pulse type modulation. Hence, the Squarer circuit only outputs a signal when the sweep oscillator output is present and the marker operation has been selected.

A8 SAMPLER, TROUBLESHOOTING

A8 Sampler component failures affect the plug-in crystal markers. On the front panel of the 8350A, select a start frequency of 10 MHz and a stop frequency of 2.4 GHz. Select 83522A 50 MHz markers (amplitude or intensity). Monitor A7TP3 and check for birdie pulses as noted in Figure 8-57 (A7 Service Sheet). If birdie pulses are present then the A8 Sampler assembly is operational and a problem exists on the A7 Marker Assembly. Refer to the troubleshooting procedure for the A7 Marker Assembly. If there are no birdie pulses then a problem exists on the A8 Sampler Assembly.

NOTE

Some distortion of the actual waveforms may occur due to probe capacitance.

Monitor A8TP1. With the selection of any internal marker, the 50 MHz output of the crystal oscillator should appear as illustrated in the lower right corner of the A8 Schematic Diagram. If the 50 MHz signal is not present, check control signal OSC EN U10 pin 2. When internal markers are selected, OSC EN will be a logical one. If OSC EN does not go high with internal markers selected, ensure that CR1 is not shorted. Also ensure that data latch U10 is operational.

To troubleshoot U10 utilize the Hex Data Rotation Write self test. To utilize the test, perform the following keystrokes on the 8350A Sweep Oscillator Mainframe:

INSTR PRESET	Initiates Instrument Preset
SHIFT 0 0	Initiates hex address mode
2 GHz s 0 2	Addresses data latch A8U10
M4	Initiates HEX DATA ROTATION WRITE

Monitor the I/O operation of U10. Check for waveforms in Figure 8-2 at the beginning of this Service Section.

If the output of crystal Y1 is present at A8TP1 and U10 is operational, check A8TP2 for the waveforms given in the lower right corner of the A8 Schematic Diagram. If no signal appears at A8TP2 for any selection of internal markers, check U7C. If the signal does not appear for 1 MHz markers, check divider U6. If a signal does not appear for either the 1MHz or 10 MHz markers, check U9. If a signal does not appear for 10 MHz markers, check CR3 and U7B. If a signal does not appear for 50 MHz markers, check CR2 and U7A.

If A8TP2 is valid and there are no internal markers, check the output of U11C and U11D. Their outputs should be a 1, 10, or 50 MHz signal, depending upon which marker is selected. Their outputs will be 180° out of phase.

If the comb generator circuitry is operational, verify that the RF output signal from directional detector DC1 is getting to the A8 assembly. Remove W6 from the J1 connector on the assembly. Select a CW frequency setting anywhere in the band. With an external power meter, measure the level of the signal at W6. The signal level should be approximately 25 dB below the level indicated on the front panel of the 83522A. If there is no signal present, or the amplitude is more than 25 dB down from the RF output, a problem exists in either the directional detector DC1, cables W8 or W6, or the connector between them. Trace the signal path to determine the failed component.

If the signal from the directional detector is valid, check Internal Mixer (E) and Programmable Low Pass Filter Circuitry (G) by monitoring A8TP3 with an oscilloscope. Set the 8350A Start/Stop sweep for 10 MHz to 2.4 GHz with a Sweep Time of 100 msec. Select 83522A 1MHz amplitude markers and set the output power to +13 dBm. Vary potentiometer R29 (1M). The envelope height should vary. Select 10 MHz markers and vary potentiometer R30 (10 MHz). The envelope height should vary. Select 50 MHz markers and vary potentiometer R31 (50 MHz). The envelope height should vary. If no effect is observed at A8TP3 for all three selected marker frequencies, suspect the internal mixer Q1 or analog switch U5. If only one of the selected marker frequencies displays improper operation then a failed component exists in Programmable Low Pass Filter (G) or possibly U5.

If A8TP3 output appears correct, check the waveform at A8TP4 for each marker position. Both waveforms appear in the lower right corner of the A8 Schematic Diagram. If the pulse amplitude is not approximately 1 volt, attempt to adjust the corresponding IF gain control. If the adjustments do not have any effect, check U5.

Reduce the RF output level from +13 to 0 dBm. The pulse amplitude should remain the same. If the amplitude varies, check the Gain Shaping Circuit (I).

If the pulses at A8TP4 appear correct, check the output of U2 pin 7 for amplified pulses. If no output is seen from U2 check that control lines L PULSE and SQ EN are both enabled.

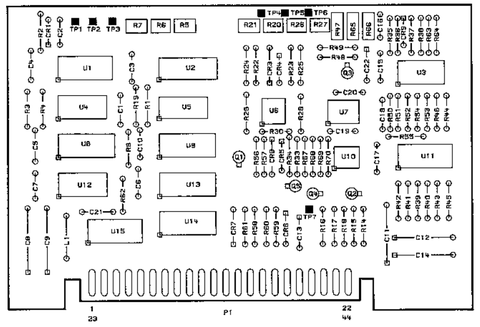


Figure 8-56. A7 Marker, Component Locations

A7P1

PIN	SIGNAL	I/O	TO/FROM	BLOCK
1 23	BIRDIE L ZMRQ	IN OUT	A8P1-1 P2-23	E E
2 24	BIRDIE RET L 10BMKR	OUT OUT	A8P1-2 A4P1-25	E E
3 25	L MKRLED L SMPLEN	OUT OUT	A2J1-10 A3P1-25	E E
4 26	L PULSE DLY COMP	OUT OUT	A8P1-23 A6P1-26	D I
5 27	YO DRIVE V +5V	IN IN	A6P1-42 A3P1-6,7	J K
6 28	−40V −15V	IN IN	P1-11 P2-28	NOT USED K
7 29	+10V SC VTUNE	IN IN	P1-8 A8P1-29	K I
8 30	GND DIG GND DIG			K K
9 31	BD1 BD0	IN IN	A3P1-9 A3P1-31	B,G B
10 32	BD3 BD2	IN IN	A3P1-10 A3P1-32	B,G B,G
11 33	BA1 BA0	IN IN	A3P1-11 A3P1-33	A A
12 34	BA3 BA2	IN IN	A3P1-12 A3P1-34	A A
13 35	BD5 BD4	IN IN	A3P1-13 A3P1-35	B,G B,G
14 36	BD7 BD6	IN IN	A3P1-14 A3P1-36	B,G G
15 37	GND ANLG GND ANLG			K K
16 38	+20V +15V	IN IN	P1-7 P2-29	NOT USED K
17 39	−10V −40V	IN IN	P1-13 P1-11	K NOT USED
18 40	L INST 1 L RFON	IN IN	A3P1-8 A2J1-38	A J
19 41	OSC BIAS L RFM	OUT IN	A12A1J1-6 P2-24	J D
20 42	L SSRO SQ MOD	IN IN	A6P1-23 P2-26	I D
21 43	L 80SW1 PULSE IN	IN	NOT USED J5(BNC)	D
22 44	L 80SW2 +5V REG	IN	NOT USED A6P1-7	K

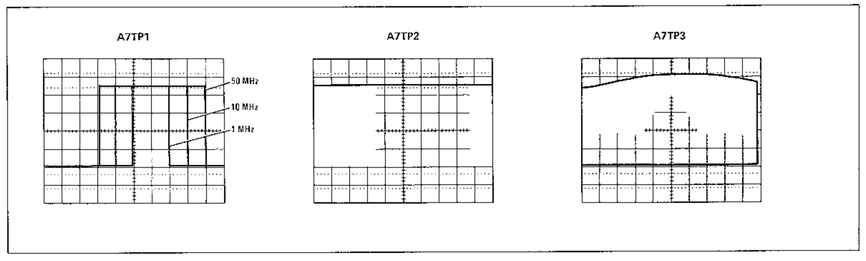


Figure 8-57. A7 Marker, Test Points 1 thru 3

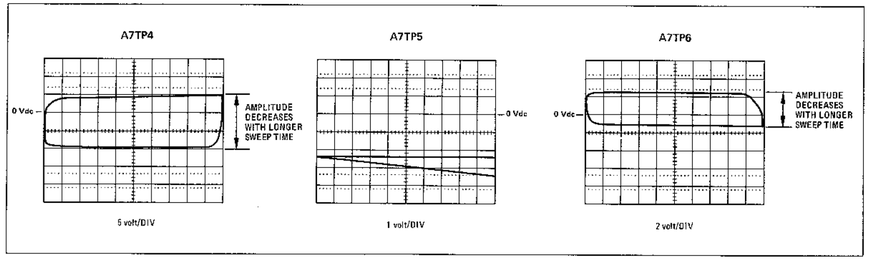


Figure 8-58. A7 Delay Compensation, Test Points 4 thru 6

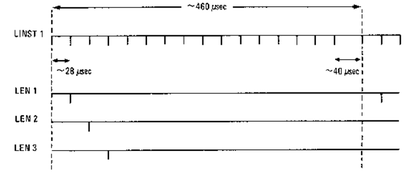


Figure 8-59. A7 Address Decoder Timing Diagram

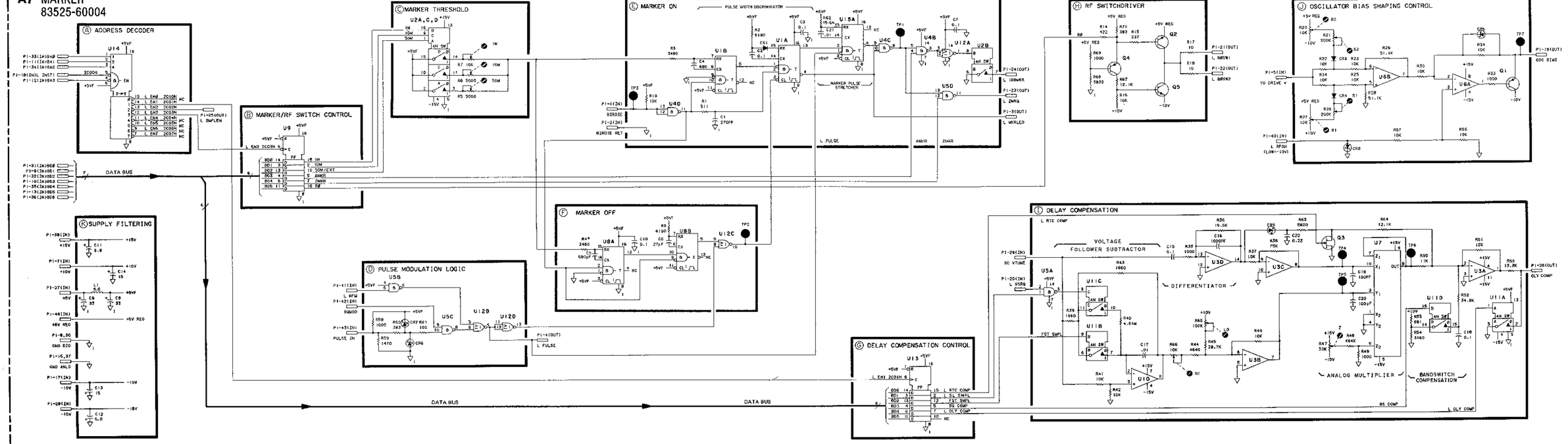
NOTES

1. THE FOLLOWING KEY ENTRIES PROVIDE FRONT PANEL ACCESS FOR A DATA WRITE/READ OPERATION TO/FROM THE ADDRESSED LOCATION:

FUNCTION	KEY ENTRY
*Hex Address Entry	SHIFT 0 0 (enter hex address)
Hex Data WRITE	M2 (enter data: two hex digits)
Hex Data READ	M3
Hex Data Rotation Write	M4
Hex Addressed Fast Read	M5

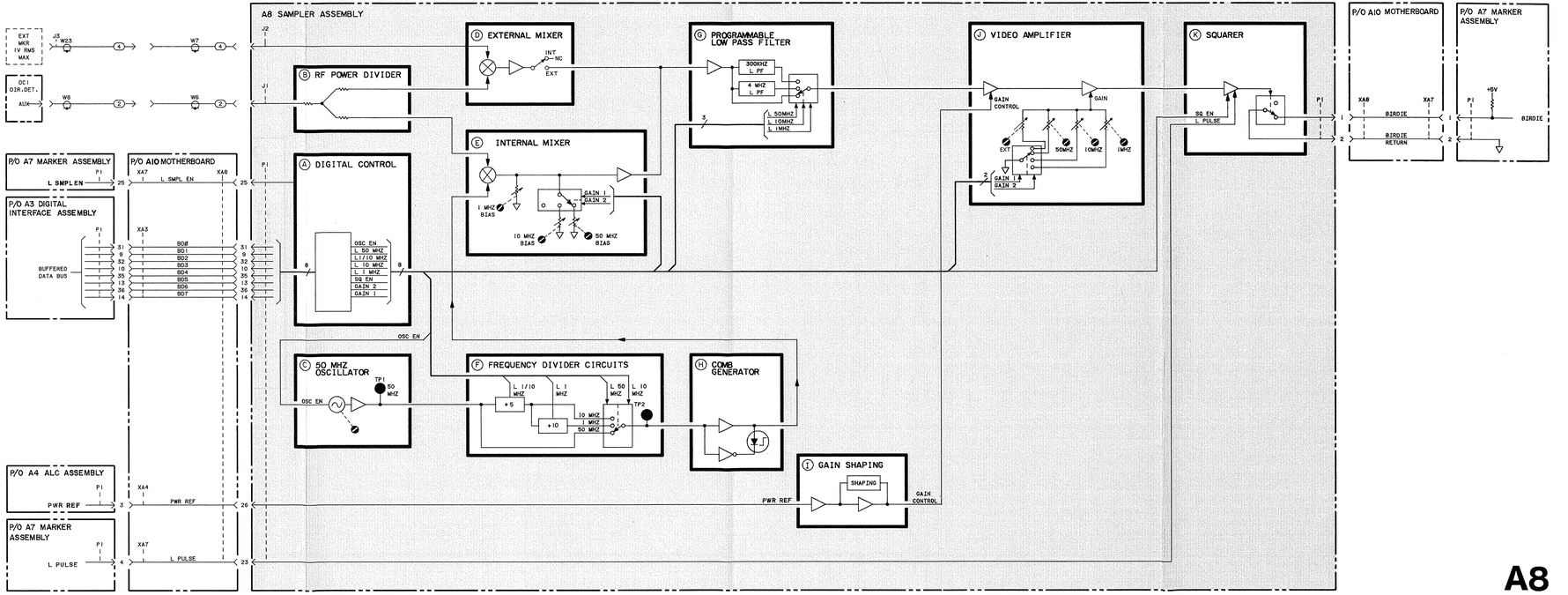
*TO ADDRESS A DIFFERENT LOCATION, PRESS M1 AND ENTER THE NEW ADDRESS, OR USE THE INCREMENT KEYS ◆ ◆ TO STEP TO THE NEW ADDRESS.

TO PREVENT THE MICROPROCESSOR FROM SERVICING THE RETRACE INTERRUPT, PRESS 8380A CW .



SERIAL PREFIX: 2040A

Figure 8-60. A7 Marker, Schematic Diagram



A8

Figure 8-61. A8 Sampler Assembly, Block Diagram

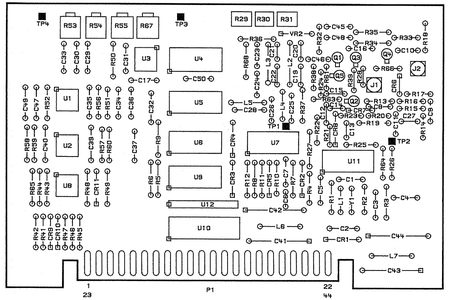
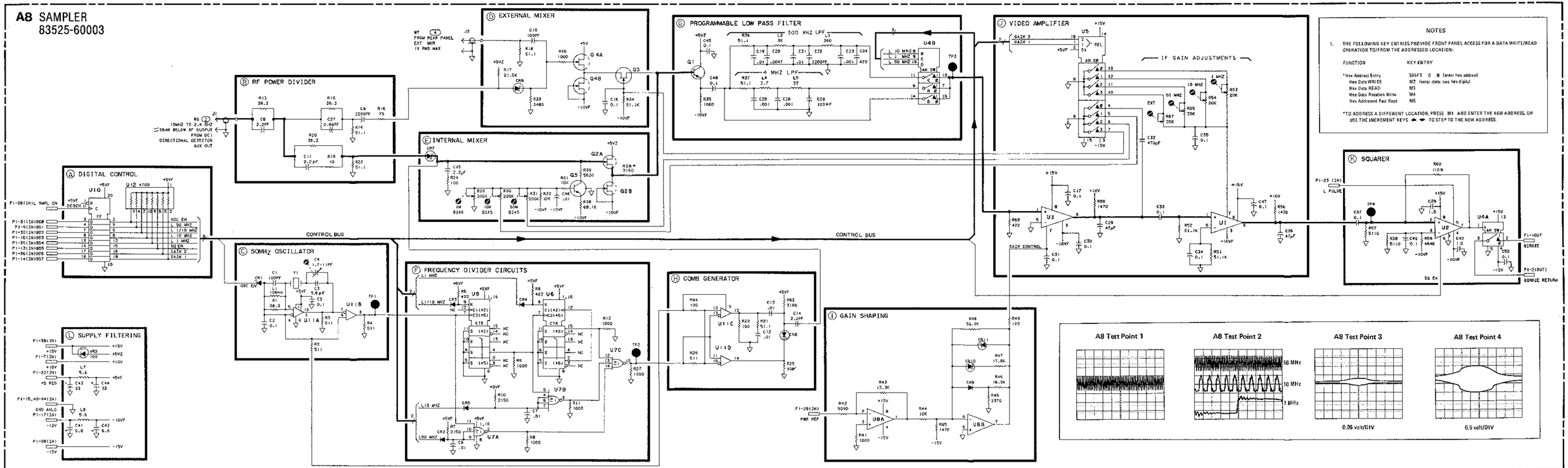


Figure 8-62. A8 Sampler, Component Locations

A8P1

PIN	SIGNAL	I/O	TO/FROM	BLOCK
1 23	BIRDIE L PULSE	OUT IN	A7P1-1 A7P1-4	K K
2 24	BIRDIE RET NC	OUT	A7P1-2	K
3 25	NC L SMPL EN	IN	A7P1-25	A
4 26	NC PWR REF	IN	A4P1-3	I
5 27	NC +5V	IN	A3P1-6,7	NOT USED
6 28	−40V −15V	IN IN	P1-11 P2-28	NOT USED L
7 29	+10V NC	IN	P1-8	L
8 30	GND DIG GND DIG			NOT USED NOT USED
9 31	BD1 BD0	IN IN	A3P1-9 A3P1-31	A A
10 32	BD3 BD2	IN IN	A3P1-10 A3P1-32	A A
11 33	BA1 BA0	IN IN	A3P1-11 A3P1-33	NOT USED NOT USED
12 34	BA3 BA2	IN IN	A3P1-12 A3P1-34	NOT USED NOT USED
13 35	BD5 BD4	IN IN	A3P1-13 A3P1-35	A A
14 36	BD7 BD6	IN IN	A3P1-14 A3P1-36	A A
15 37	GND ANLG GND ANLG			L NOT USED
16 38	+20V +15V	IN IN	P1-7 P2-29	NOT USED L
17 39	−10V −40V	IN IN	P1-13 P1-11	L NOT USED
18 40	L INST1 GND ANLG	IN	A3P1-8	NOT USED L
19 41	NC GND ANLG			L
20 42	NC GND ANLG			L
21 43	NC GND ANLG			L
22 44	+5V REG GND ANLG	IN	A9P1-7	L L



SERIAL PREFIX: 2040A

Figure 8-63. A8 Sampler, Schematic Diagram

RF SECTION, CIRCUIT DESCRIPTION

The RF Section includes the high-frequency microcircuits, with their bias boards, that produce the actual RF output power. These components include A12, A14 through A17, A19, and DC1. All other plug-in assemblies function essentially to control these RF components. The connections between microcircuits and other assemblies are provided on the Overall Block Diagram. Refer to the Overall Block Diagram circuit description for a more general, functional description.

NOTE

Assembly circuit descriptions are discussed in signal flow order.

A12 YIG Oscillator

The A12 YIG (Yttrium-Iron-Garnet) Oscillator (YO) is the solid-state tunable microwave source. Its output frequency ranges from 3.81 to 6.2 GHz, with approximately +12 to +14 dBm of output power. The oscillator's resonant tank circuit is basically a small YIG sphere with a resonant frequency which depends on the surrounding magnetic field strength. The magnetic field is established by an opposing pair of electromagnetic "main coils." Changing the current through the coils changes the magnetic field strength, and hence the frequency of oscillation. The sphere is lightly coupled to a bi-polar transistor, providing the gain necessary to sustain oscillation. A FET amplifier provides the final output power gain.

The A12A1 YO Bias assembly supplies the biasing for the oscillator and YO amplifier. This board is matched to the YO, and cannot be separately replaced. There is a single adjustment (R4) on the assembly, optimizing the FET gate bias for minimum harmonics in higher frequency, multiband RF plug-ins. R4 does not need to be adjusted in the 83522A. The bias assembly provides zener protection against high-voltage transients that appear across the main coils. It also supplies current for a resistive heater that helps maintain the oscillator at a constant temperature.

The dynamic response of the YO (i.e. how fast frequency changes for a fast change in coil current) is somewhat limited, due to the inductive and magnetic delays of the electromagnet coils and poles. Delay compensation circuits help during a sweep, but frequency modulation is limited to low modulation frequencies. To allow high-frequency modulation, a smaller, faster, air-core FM coil is added to the YO. Its magnetic field adds to the main coil's field, yet frequency changes are far quicker.

A17 Modulator/Mixer

The A17 Modulator/Mixer mixes a fixed 3.8 GHz signal with the swept 3.81 to 6.2 GHZ YO output, producing the 0.01 to 2.4 GHz RF output. The swept YO output acts as the Local Oscillator signal for the mixer. The internal PIN diode modulator attenuates the fixed 3.8 GHz input, providing both amplitude leveling and pulse modulation. The mixer has a high conversion loss, and produces approximately −20 dBm of mixed output with +9 dBm of 3.8 GHz input and no modulator attenuation.

A16 Cavity Oscillator

The A16 Cavity Oscillator provides a fixed 3.8 GHz RF output at approximately +9 dBm which is mixed down by the swept YO output, yielding the heterodyned low-frequency output. This source is extremely stable in both frequency and amplitude. The +20V and −10V lines provide power for the A16 assembly. Two large, separately-replaceable capacitors help filter these supplies to reduce residual FM noise.

A14 Amplifier

The A14 Amplifier provides approximately 40 dB of gain from 0.01 to 2.4 GHz. The amplifier gain drops sharply at higher frequencies, providing a lowpass nature which rejects the unwanted mixing products.

The A14A1 Amplifier Bias assembly provides the various bias currents for the A14 amplifier. It is matched and attached to the microcircuit at the factory, has no adjustments or replaceable parts, and cannot be replaced separately as an assembly. The +20V and L RFON lines provide the power. When the RF is "off," the bias is removed, shutting off the amplifier completely.

A15 DC Return

The A15 DC Return is simply a shunt RF choke. The shunt inductor allows DC currents to flow to ground while passing on the RF power with less than 0.6 dB of insertion loss.

DC1 Directional Detector

The DC1 Directional Detector serves two purposes: 1) detects the RF power amplitude; and 2) samples a portion of the RF energy for use in the marker circuits. The insertion loss for the entire package is less than 3.5 dB.

A simple resistive directional bridge samples a portion of the RF energy to a diode detector. The RF is rectified and filtered, providing a voltage, proportional to the peak RF amplitude, which is used for leveling. A single resistor (A10R1) biases the detector diode through feed-through E1. Feed-through E2 carries the detected signal, but also carries a second bias current from the A4 assembly for a second, temperature compensating diode. An internal resistor helps protect the static sensitive diodes.

A simple resistive tap samples a portion of the RF frequency for use in the marker generation circuits. The SAMPLED RF output is aproximately 25 dB below the front panel output power, and ranges from 0.01 to 2.4 GHz.

A19 Step Attenuator (Option 002 Only)

On RF plug-ins equipped with Option 002, the A19 Step Attenuator provides up to 70 dB of attenuation in 10 dB steps. Combined with the range of the ALC loop, this yields a leveled power range of +13 to −72 dBm. The Step Attenuator consists of three fixed attenuators, with 10, 20, and 40 dB of attenuation each. Latching relays close contacts which either insert these attenuators into the RF path or bypass them. The control and drive circuitry for the attenuator is located on the A2 Front Panel Interface assembly. The insertion loss, with 0 dB attenuation selected, is approximately 0.5 dB.

RF OUTPUT Connector

On Standard or Option 002 instruments, the RF output is directed to a female type N "RF OUTPUT" connector at the front panel. On plug-ins with Option 004 (with or without Option 002), the output is directed to the rear panel RF OUTPUT connector.

RF PATH TROUBLESHOOTING

NOTE

Many RF path failure symptoms are closely related to A4 ALC failures. Refer to A4 Troubleshooting for additional information.

The RF Path consists of the microcircuits and their bias boards that produce the actual front-panel RF output. These microcircuits are sealed, cannot be repaired, and are costly to replace. Ensure that associated control circuits (i.e. the other printed circuit boards) are working correctly before replacing any microcircuit components. When certain of a failure in the RF components, isolate the problem to a single microcircuit assembly.

Three RF assemblies have bias boards attached directly to the microcircuit packages:

- The A14 Amplifier is directly attached to its bias board. The A14A1 Amplifier Bias assembly cannot be repaired, is not separately replaceable, and is supplied with the A14 microcircuit.

- The A12A1 YO Bias assembly includes two factory select resistors matched to the A12 YIG Oscillator. The bias board is part of the A12 assembly and cannot be separately replaced. If a bias board component (e.g. protection diode or variable resistor) has been externally damaged, it is acceptable (and economical) to replace that individual component. However, a bias board failure often indicates a failure inside the microcircuit and may require that the entire assembly be replaced.

WARNING

Many microcircuits are extremely sensistive to static electric discharges (more so when the microcircuits are removed from their bias boards or control circuits).

Before handling a microcircuit, discharge your own body by touching the instrument chassis or microcircuit package. Avoid touching the center conductors of the RF connectors and bias feed-throughs at all times.

Microcircuits should be stored and transported in static-protective packaging. Never package microcircuits with styrofoam, cellophane (unless treated for static), or adhesive tape.

Do not attempt to test any microcircuits, at a bias feed-through or the RF connectors, with an ohmmeter. Resistance measurements are rarely useful, and will often destroy a working microcircuit. Measure DC voltages at the bias feed-throughs with a high-impedance DC voltmeter only with bias or control connections intact.

The following troubleshooting procedure traces power levels through the RF path. RF measurements should be made with a high-frequency spectrum analyzer or an RF power meter. A type-N (female)-to-SMA adapter, along with a short, flexible RF cable terminated at both ends with SMA male connectors, will make troubleshooting easier.

Opening RF connections within the ALC loop will cause the loop to be unleveled, producing abnormally high power levels (up to +20 dBm) and harmonic distortion. The ALC loop includes all connections between the A17 Mod/Mix and DC1 Directional Detector. (Figure 8-25, within the A4 Troubleshooting section, provides a graphic definition of the loop.) If necessary, the modulators may be externally biased using the Open Loop Procedure described in the A4 Troubleshooting Section. If possible, avoid opening the ALC loop to make RF measurements. In any case, it is a good idea to begin troubleshooting just outside the ALC loop.

Failure Symptoms

The information below should be used to help systematically troubleshoot to the individual RF assembly. Based on the failure symptom, the components most likely to have failed are listed, with the most probable failure cited first. Hints for ensuring that the RF Path is actually responsible for the failure are also given. For troubleshooting information related to a specific assembly, refer to **Microcircuit Verification By Assembly** below.

NOTE

All references to test points, pin connections, etc., can be located on the RF Schematic, Figure 8-66.

NO RF POWER

- A12 YIG OSCILLATOR. Check power supplies and bias levels. OSC BIAS (TP "ON") should be at −10 Vdc, with some shaping. TP "G" should be approximately −2 Vdc. Check TP "M" for the waveform entitled EMITTER/COIL, Figure 8-48, within the A6 Service Sheet. This waveform represents the current across the main coil. Check the RF output directly at the YO for approximately +14 dBm at several frequencies.

- A14 AMPLIFIER. Check power supplies. Check the power directly out of A14. This will open the ALC loop. Expect to measure approximately +20 dBm unleveled RF output with high harmonic distortion. If this is undesirable, refer to A4 troubleshooting and follow the Open Loop Procedure to externally level the RF while opening the ALC loop.

- A17 MOD/MIX. If A17 is suspected, remove the A4 assembly. This removes all modulator current and provides an unrestricted path for RF. If full unleveled RF power is achieved, refer to A4 Troubleshooting. If power is still bad, disconnect W25 and check the RF output directly out of the mixer (open loop power should measure approximately −12 dBm). Before replacing this assembly, ensure that A16 Cavity Oscillator is functioning properly.

- A16 CAVITY OSCILLATOR. Check power supplies. Check RF output for approximately +9 dBm at 3.8 GHz.

MAXIMUM RF UNLEVELED POWER

- Refer to this symptom under A4 Troubleshooting.

- DC1 DIRECTIONAL DETECTOR. Select a CW frequency anywhere in the band. Verify maximum unleveled RF output power. Check INT DET 0 output to be equal to or more negative than −0.2 Vdc. (It may be necessary to perform INT DET 0 BIAS adjustment. Refer to Section V, Adjustments.) For more information refer to A4 Troubleshooting.

- A17 MOD/MIX. Check modulator bias line MOD 0. It should be slightly negative. If it is approximately +4 Vdc while A4TP6 is approximately +7.5 Vdc, the modulator diode is probably open. If MOD 0 is at 0.0 Vdc, but A4TP6 is at +7.5 Vdc, troubleshoot the A4 PIN Mod 0 Driver and connections to the modulator.

HARMONIC DISTORTION

- A12 YIG OSCILLATOR. If harmonics are unacceptable, check the spectral purity of the YO output. If harmonics are less than 14 dB below the fundamental, replace A12.

- A14 AMPLIFIER. Check the power level into A17 Mod/Mix, and trace the problem back through the RF path if it is too low. Measuring power or spectral content directly out of A17 or A14 will open the ALC loop, causing maximum unleveled power and high harmonic distortion even without a failure. Refer to A4 Troubleshooting and perform the Open Loop Procedure. This procedure externally biases the modulator to level RF power while the ALC loop is open.

SPURIOUS DISTORTION

- A17 MOD/MIX. Select a CW frequency anywhere in the band and check RF output for spurs 3.8 GHz removed from the carrier. The mixer may be leaking the swept LO frequency (3.81 − 6.2 GHz). However, the A14 Amplifier should filter these out.

POWER DROP-OUTS

- A12 YIG OSCILLATOR. If power is present and leveled across part of either band, but drops out entirely for the rest of the band, suspect A12. Check OSC BIAS for approximately −10 Vdc. Check the RF power directly out of the YO. If it appears to be faulty refer to Section V, Adjustments, and perform the A7 Oscillator Bias adjustments.

POWER HOLES

- Check all RF connections in the proper loop(s). Narrow-band power dips or "holes" are usually the result of loose or faulty RF connections. Tighten all internal RF connectors. Secure the front-panel RF connection. Inspect the front-panel RF connector for damage or wear, and clean or replace parts as necessary. Section VI, Replaceable Parts, provides an exploded view of the RF connector.

Microcircuit Verification By Assembly

The information below is organized by microcircuit assembly in RF signal flow order. It provides troubleshooting tips to isolate a particular microcircuit failure. This information is intended as a guide. Any suspected failure should be thoroughly researched before replacements are made.

The general approach to troubleshooting is:

1. Make sure that all power supply voltages are present. If not, trace the problem back through the 83522A to the 8350A.

2. Make sure all bias and control signals are present. If not, trace the problem back to the supplying assemblies.

3. Check the RF levels into the suspected microcircuit. If faulty, trace the problem back through the RF path.

4. Check the RF levels out of the suspected microcircuit. If faulty, replace the assembly.

IN EVERY CASE, check power supply voltages. Make sure control signals and bias voltages are being supplied from the other circuits before replacing any microcircuit. Refer to the Service Sheet appropriate to the assembly supplying the control signals for voltage levels and waveforms.

A12 YIG OSCILLATOR

Check RF output directly from the YO for about +14 dBm. For power drop-outs, check OSC BIAS for −10 Vdc

A16 CAVITY OSCILLATOR

The output of this assembly should measure approximately +9 dBm RF power at 3.8 GHz.

A17 MODULATOR/MIXER

Ensure that A16 is functioning. Control line MOD 0 should be near +0.7 Vdc. If not, remove the modulation control wire and check for approximately +5 Vdc. If this is not the case, troubleshoot A4. To verify the MOD/MIXER, remove the A4 assembly. Monitor the RF output directly from A17. In this open loop condition the power should measure approximately −12 dBm. (Expect high harmonic distortion.)

A14 AMPLIFIER

Check for power input as described under A17, above. Verify RF output at approximately +20 dBm unleveled with high harmonic distortion. When trying to isolate harmonic sources, refer to A4 Troubleshooting and follow the Open Loop Procedure. This procedure externally biases the modulators to level the RF power under open loop conditions.

A15 DC RETURN

An A15 failure is extremely unlikely. However, this component can be tested OUT OF CIRCUIT with an ohmmeter. Verify DC short to ground.

DC1 DIRECTIONAL DETECTOR

Check for approximately +15 dBm of leveled output power. Ensure that power is nominally +13 dBm and check the detector output, E2, for approximately −0.2 Vdc or more negative. If temperature drift is suspected, check that the INT DET 0 BIAS adjustment (A4R4) has an effect on the detected output level. If it does not, replace DC1.

A19 STEP ATTENUATOR (Option 002 Only)

Check the output of DC2 for approximately +13 dBm. Verify that A3 Configuration Switch is set for Option 002 (see A3 Service Sheet, Table 8-8). Set the 8350A front panel step keys, ▲ ▼, for 10 dB steps. Increment the power setting with the step keys to run the attenuator through its 70 dB range. (Power meters will typically NOT have the dynamic range to verify this operation.) The control circuits can be manually exercised by operating the sweep oscillator in the CW mode and performing a Hex Data Write to address 2F00. Enter two hex digits in the format "0x", where 00 equates with 0 dB attenuation, 01 with 10 dB attenuation, 02 with 20 dB attenuation, and so on.

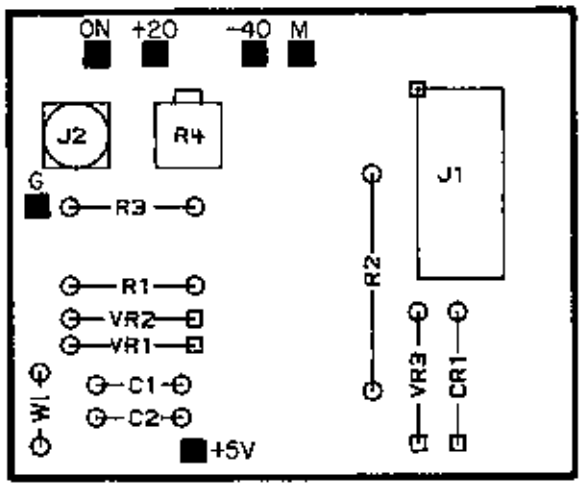


Figure 8-64. A12A1 YO Bias, Component Locations

RF SCHEMATIC DIAGRAM

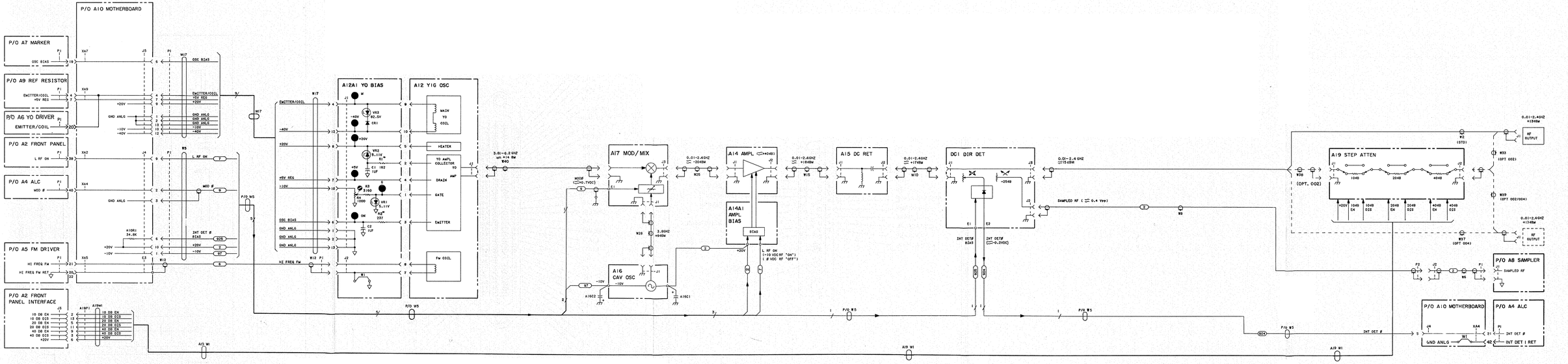


Figure 8-65. RF Schematic Diagram

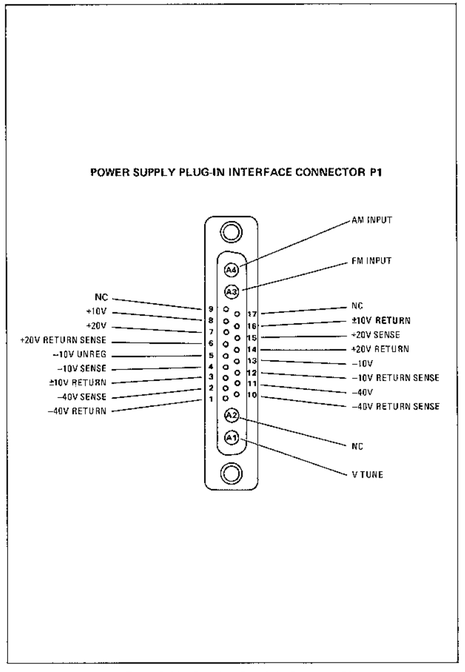


Figure 8-66. Interface Signals in Connector P1

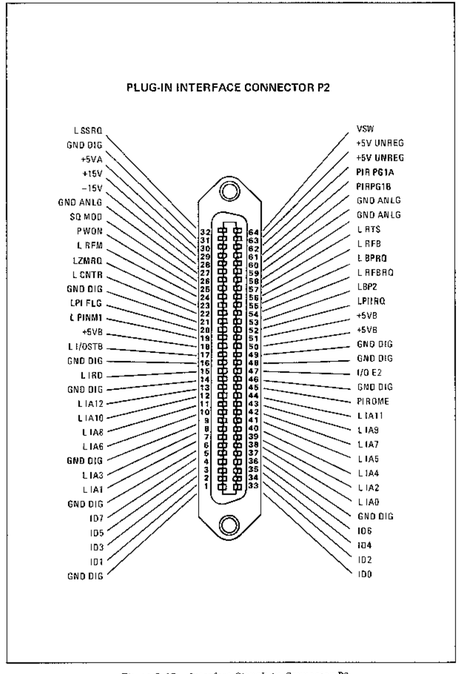


Figure 8-67. Interface Signals in Connector P2

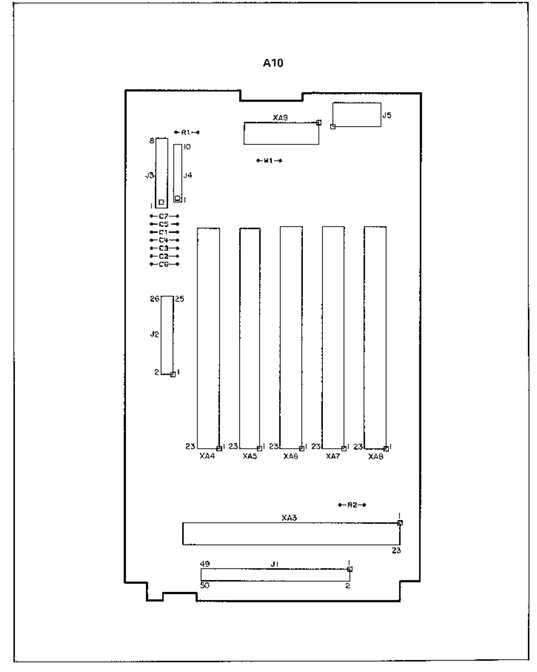


Figure 8-68. A10 Motherboard, Component Locations

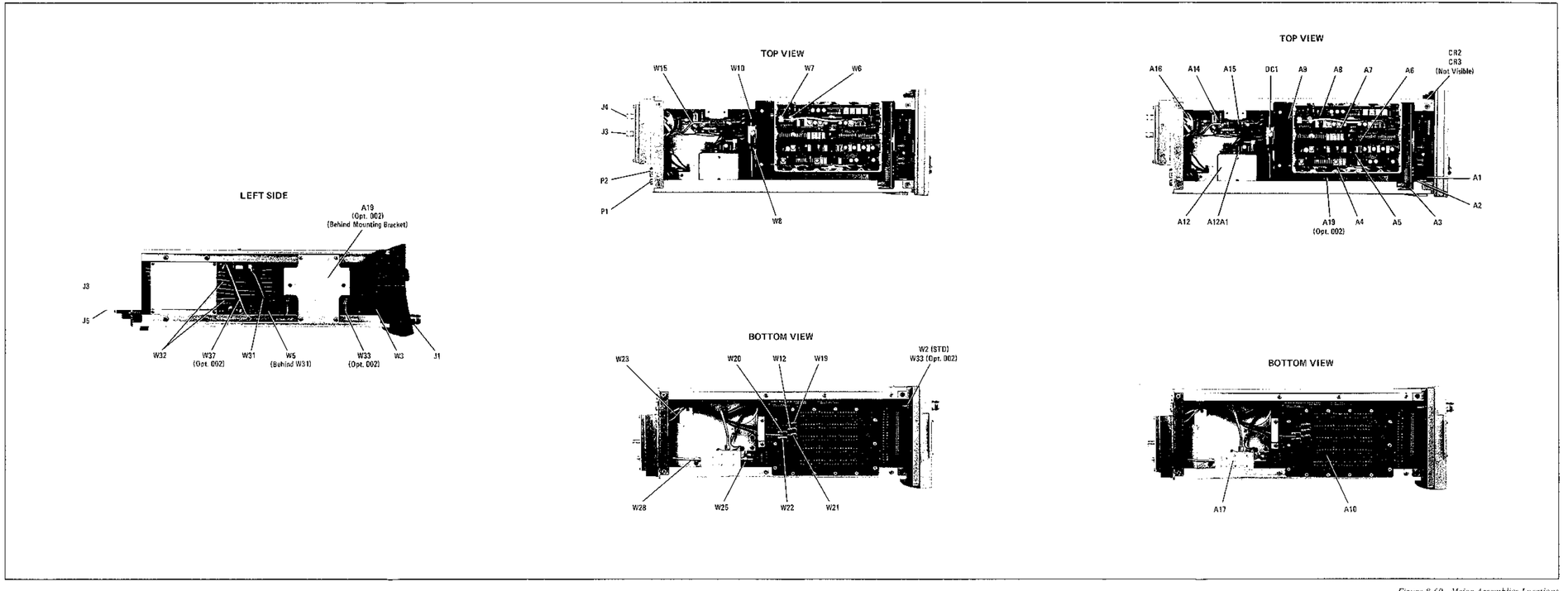


Figure 8-69. Major Assemblies Locations

Mnemonic	Signal Source	Mnemonic Description	Power Supply Interface P1	Plug-in Interface P2	Dig Interface A3P1	Dig Interface A3J1	ALC A4P1	FM A5P1	YO A6P1	Marker A7P1	Sampler A8P1	Ref Resistor A9P1	F.P. Interface A10J1	P/O Plug-in Interface A10J2	Power Supply Interface A10J3	RF Wiring Harness A10J4	RF Ribbon Cable A10J5	Miscellaneous
AM	P1-A4	Amplitude Modulation	A4-C[1]				4											E4-C[1]
BASE	A6P1-22	YO Current Drive Control							22			1						
L B0SW1	A7P1-21	RF Switch, −10V=Band 0 (Not Used)								21*						7		
L B0SW2	A7P1-22	RF Switch; 10V=Band 0 (Not Used)								22*						8		
BA0	A3P1-33	Buffered Addr 0			33		33	33	33	33	33*		11					
BA1	A3P1-11	Buffered Addr 1			11		11	11	11	11	11*							
BA2	A3P1-34	Buffered Addr 2			34		34	34	34	34	34*							
BA3	A3P1-12	Buffered Addr 3			12		12	12	12	12	12*							
BD0	A3P1-31	Buffered Data 0			31		31	31	31	31	31		5					
BD1	A3P1-9	Buffered Data 1			9		9	9	9	9	9		3					
BD2	A3P1-32	Buffered Data 2			32		32	32	32	32	32		7					
BD3	A3P1-10	Buffered Data 3			10		10	10	10	10	10		9					
BD4	A3P1-35	Buffered Data 4			35		35	35	35	35	35		15					
BD5	A3P1-13	Buffered Data 5			13		13	13	13	13	13		13					
BD6	A3P1-36	Buffered Data 6			36		36	36	36	36	36		19					
BD7	A3P1-14	Buffered Data 7			14		14	14	14	14*	14		17					
BIRDIE	A8P1-1	Marker Birdie								1	1							
BIRDIE RET	A8P1-2	Marker Birdie Return								2	2							
L BPRQ	A6P1-2	L=Blanking Pulse Request							2*					4				
L CNTR	P2-22	L=Counter Trigger (Not Used)		22														
COLLECTOR	A9P1-2	Ref Resistor Sense							41			2						
DET REF	A4P1-40	Detected Power Reference (Not Used)					40											
DLY COMP	A7P1-26	YO Delay Compensation							26	26								
EMITTER/COIL	A9P1-4	YO Coil Current							20			4					4	
EXT CAL	A10J1-41	External Leveling Power Cal					24						41					
EXT DET	A10J1-47	External Leveling Input					23						47					
EXT DET RET	A10J1-43	External Leveling Return					1						43					
FLAG	A10J1-31	Front Panel Flag			42								31					
FM IN	P1-A3	Frequency Modulation Input	A3-C[1]					40										E1-C[1]
FM IN RET	P1-A3	Frequency Modulation Return	A3-S[2]					39,41										E1-S[2]

[1] Coaxial Cable - Center conductor
[2] Coaxial Cable - Shield
* Not used on this assembly

Table 8-13. 83522A Motherboard Wiring List (1 of 5)

Mnemonic	Signal Source	Mnemonic Description	Power Supply Interface P1	Plug-in Interface P2	Dig Interface A3P1	Dig Interface A3J1	ALC A4P1	FM A5P1	YO A6P1	Marker A7P1	Sampler A8P1	Ref Resistor A9P1	F.P. Interface A10J1	P/O Plug-in Interface A10J2	Power Supply Interface A10J3	RF Wiring Harness A10J4	RF Ribbon Cable A10J5	Miscellaneous
L FP1	A3P1-15	L=F.P. Display Write			15								21					
L FP2	A3P1-37	L=F.P. Keyboard Read			37								23					
L FP3	A3P1-16	L=F.P. Annunciator Write			16								25					
L FP4	A3P1-26	L=F.P. Annunciator Write			26								6					
L FP5	A3P1-30	L=F.P. RF Control			30								1					
FREQ CAL	A10J1-37	Band 0 Freq Cal							4				37					
FREQ TRK V	A10J1-36	Frequency Tracking Voltage					26	24					36					
HI FREQ FM	A5P1-21	YO FM Coil Drive						21										E3-C[1]
HI FREQ FM RET	A5P1-20,22	YO FM Coil Return						20,22										E3-S[2]
L IA0	P2-38	Instr Bus - Inv Addr 0		38		12												
L IA1	P2-7	Instr Bus - Inv Addr 1		7		13												
L IA2	P2-39	Instr Bus - Inv Addr 2		39		14												
L IA3	P2-8	Instr Bus - Inv Addr 3		8		15												
L IA4	P2-40	Instr Bus - Inv Addr 4		40		16												
L IA5	P2-41	Instr Bus - Inv Addr 5		41		18												
L IA6	P2-10	Instr Bus - Inv Addr 6		10		19												
L IA7	P2-42	Instr Bus - Inv Addr 7		42		20												
L IA8	P2-11	Instr Bus - Inv Addr 8		11		21												
L IA9	P2-43	Instr Bus - Inv Addr 9		43		22												
L IA10	P2-12	Instr Bus - Inv Addr 10		12		23												
L IA11	P2-44	Instr Bus - Inv Addr 11		44		24												
L IA12	P2-13	Instr Bus - Inv Addr 12		13		25												
ID0	P2-33	Instr Bus - Data 0		33		2												
ID1	P2-2	Instr Bus - Data 1		2		3												
ID2	P2-34	Instr Bus - Data 2		34		4												
ID3	P2-3	Instr Bus - Data 3		3		5												
ID4	P2-35	Instr Bus - Data 4		35		6												
ID5	P2-4	Instr Bus - Data 5		4		7												
ID6	P2-36	Instr Bus - Data 6		36		8												
ID7	P2-5	Instr Bus - Data 7		5		9												

[1] Coaxial Cable - Center conductor
[2] Coaxial Cable - Shield
* Not used on this assembly

Table 8-13 83522A Motherboard Wiring List (2 of 5)

Mnemonic	Signal Source	Mnemonic Description	Power Supply Interface P1	Plug-in Interface P2	Dig Interface A3P1	Dig Interface A3J1	ALC A4P1	FM A5P1	YO A6P1	Marker A7P1	Sampler A8P1	Ref Resistor A9P1	F.P. Interface A10J1	P/O Plug-in Interface A10J2	Power Supply Interface A10J3	RF Wiring Harness A10J4	RF Ribbon Cable A10J5	Miscellaneous
L INST1	A3P1-8	L=Plug-in Control			8		18	5		18	18*							
L INST2	A3P1-29	L=Plug-in Control			29				18									
INT DET Ø	A10J4-5	Band Ø RF Detector					21									5		
INT DET Ø BIAS	A10R1	Band Ø Detector Bias														6		R1
INT DET 1 RET	CR1	Band 1 RF Detector (Not Used)					20*											E2-C[1]
INT DET RET	CR1	Band 1 RF Detector Return (Not Used)					42*											E2-S[2]
I/O E2	P2-47	Plug-in I/O Enable		47		30												
L I/OSTB	P2-17	Inv I/O Strobe		17		33												
L IRD	P2-15	L=Instr Bus Read		15		29												
LO FREQ FM	A5P1-2	Low Freq FM (Main Coil)						2	25									
L MKRLED	A7P1-3	L=Marker LED								3			10					
MOD Ø	A4P1-44	Band Ø RF Modulation					44									2		
MOD 1	A4P1-19	Band 1 RF Modulation (Not Used)					19*										15	
MOD DRIVE	A4P1-22	Modulator Drive (Not Used)					22											
OSC BIAS	A7P1-19	YIG Oscillator Bias								19							6	
L PIFLG	A3J1-39	L=Plug-in Flag		20		39												
L PIIRQ	A3J1-40	L=Plug-in Interrupt Request		52		40												
L PINMI	INCI	L=Plug-in Non-Maskable Interrupt		19														
PIROME	P2-45	Plug-in ROM Enable		45		26												
PIRPGA	A10J1-35	Plug-in RPG A		60									35	14				
PIRPGB	A10J1-34	Plug-in RPG B		61									34	16				
PULSE IN	J5(BNC)	External Pulse Input								43								E6-C[1]
L PULSE	A7P1-4	L=Pulse Mod					41			4	23						16	
PWON	P2-25	Power On		25	22				15				29	7				
PWR REF	A4P1-3	Power Level Reference					3				26							
PWR SW/COMP	A5P1-23	Power Sweep, Level Compensation					5	23										
L RFB	P2-56	L=RF Blanking		56			29							6				
L RFBRQ	A6P1-24	L=RF Blanking Request		54					24*					2				
L RFM	P2-24	L=RF Marker		24						41				5				
L RFON	A10J1-38	10V=RF On, 0V=RF Off								40			38			9		
L RTS	P2-57	L Retrace Strobe		57					1				4	8				

[1] Coaxial Cable - Center Conductor

[2] Coaxial Cable - Shield

* Not used on this assembly

Table 8-13. 83522A Motherboard Wiring List (3 of 5)

Mnemonic	Signal Source	Mnemonic Description	Power Supply Interface P1	Plug-in Interface P2	Dig Interface A3P1	Dig Interface A3J1	ALC A4P1	FM A5P1	YO A6P1	Marker A7P1	Sampler A8P1	Ref Resistor A9P1	F.P. Interface A10J1	P/O Plug-in Interface A10J2	Power Supply Interface A10J3	RF Wiring Harness A10J4	RF Ribbon Cable A10J5	Miscellaneous
SCAN CLK	A3P1-38	F.P. Scan Clock			38								27					
SC VTUNE	A6P1-29	Scaled Tune Voltage							29	29								
L SIRQ	A6P1-3	L=Sweep Interrupt Request			18				3									
L SMPLEN	A7P1-25	L=Sampler Latch Enable								25	25							
SQMOD	P2-26	Square Modulation (27.8/11.0 kHz)		26						42				9				
L SSRQ	A6P1-23	L=Stop Sweep Request		32					23*	20				21				
L UNLVL	A4P1-2	L=Unleveled					2		40				12					
VSW	P2-64	Sweep Voltage		64				25						22				
VTUNE	P1-A1	Tune Voltage	A1-C[1]						44									E5 C[1]
VTUNE RET	P1-A1	Tune Voltage Return	A1-S[2]						43									E5-S[2]
YO DRIVE V	A6P1-42	YO Drive Voltage							42	5			39					
L ZMRQ	A7P1-23	L=Intensity Marker Request		23						23				3				
L 10DBMKR	A7P1-24	L=10dB Amplitude Marker					25			24								
1V/GHZ	A10J1-50	1V per GHz Output											50	23				J4IBNCI
-10V REF	A6P1-5	-10V Reference Voltage					43		5									
+20V FREQ REF	A9P1-5	+20V Frequency Reference Sense							21			5						

[1] Coaxial Cable - Center Conductor

[2] Coaxial Cable - Shield

* Not used on this assembly

Table 8-13. 83522A Motherboard Wiring List (4 of 5)

Mnemonic	Signal Source	Mnemonic Description	Power Supply Interface P1	Plug-in Interface P2	Dig Interface A3P1	Dig Interface A3J1	ALC A4P1	FM A5P1	YO A6P1	Marker A7P1	Sampler A8P1	Ref Resistor A9P1	F.P. Interface A10J1	P/O Plug-in Interface A10J2	Power Supply Interface A10J3	RF Wiring Harness A10J4	RF Ribbon Cable A10J5	Miscellaneous
+20V +20V RET +20V RET SENSE +20V SENSE	P1-7 P1-14 P1-6 P1-15	+20V Regulated +20V Return +20V Return Sense +20V Sense	7 14 6 15				16*	16*	16	16*	16*	3,11	42		3 6	10	9	C7,R1
+15V	P2-29	+15V Regulated		29			38	38	38	38	38			15				C6
+10V +10/ -10V RET	P1-8 P1-3, 16	+10V Regulated +/ -10V Return	8 3				7	7	7	7	7		46		2		5,11	C5
+5V +5VA +5VB	A3P1-6,7 P2-30 P2-18,50,51	+5V Internal for RF Plug-in +5V for 8350A +5V for RF Plug-in		30 18,50,51	6,7	35, 36, 38	27	27	27	27	27*		2					
+5V REG +5V UNREG	A9P1-7 P2-62, 63	+5V Regulated +5V Unregulated		62, 63						44	22	7 12		18,20			7	C4
-10V -10V RET SENSE -10V SENSE -10V UNREG	P1-13 P1-12 P1-4 P1-5	-10V Regulated -10V Return Sense -10V Sense -10V Unregulated	13 12 4 5				17	17	17	17	17		40		5	1	10	C3
15V	P2-28	15V Regulated		28			28	28	28	28	28			13				C2
-40V -40V REF -40V RET SENSE -40V SENSE	P1-11 P1-1 P1-10 P1-2	-40V Regulated -40V Return -40V Return Sense -40V Sense	11 1 10 2				6*, 39		6, 39	6*, 39*	6*, 39*				7		12	C1
GND ANLG	P2-27,58,59	Analog Ground					15, 37	15*, 37	19, 37	15, 37	15,37* 40,41,42, 43,44	6	48	10,11,12	8	3, 4	1, 2, 13	C1-C7,R2,W1 E1-S[2], E5-S[2]
GND DIG	P2-1, 6, 14, 16,21,31,37, 46, 48, 49	Digital Ground		1, 6, 14, 16, 21, 31, 37, 46, 48, 49	4, 6	1,10,11, 17,27,28, 31,32,34, 41	8, 30	8, 30	8, 30	8, 30	8*, 30*		8					R2

[1] Coaxial Cable - Center Conductor

[2] Coaxial Cable - Shield

* Not used on this assembly

Table 8-13. 83522A Motherboard Wiring List (5 of 5)

Table 8-14. HP 83522A Cable List (Sheet 1 of 2)

Cable	Description	Connections
W1	Not Assigned	
W2	Cable Assembly, Rigid, RF OUTPUT	DC–Directional Coupler J1–Front Panel RF OUTPUT (Type N)
W3	Cable Assembly, Ribbon, Front Panel	A10J1–Motherboard A2J1–Front Panel
W4	Not Assigned	
W5	Wire Assembly, RF Section	A10J4 Motherboard A14A1, A16, A17, DC1 (RF Section)
W6	Cable Assembly, Coax, Red	W8P1–Shield Cage A8J1–Sampler Board (Sampled RF)
W7	Cable Assembly, Coax, Yellow	W23P1–Shield Cage A8J2–Sampler Board (EXT MKR)
W8	Cable Assembly, Coax, Red	DC1–Dir. Detector (Sampled RF) W6J1–Shield Cage
W9	Not Assigned	
W10	Cable Assembly, Rigid, RF	A15–DC Return DC1–Directional Detector
W11	Not Assigned	
W12	Cable Assembly, Coax, Blue	A10E3–Motherboard A12A1J2–YO (FM Coil)
W13	Not Assigned	
W14	Not Assigned	
W15	Cable Assembly, Rigid, RF	A14–Amplifier (0.01 to 2.4 GHz) A15–DC Return
W16	Not Assigned	
W17	Cable Assembly, Ribbon, RF Section	A10J5–Motherboard A12A1J1–YO
W18	Not Assigned	
W19	Cable Assembly, Coax, Green, FM IN	P1-A3–Rear Panel Interface A10E1–Motherboard
W20	Cable Assembly, Coax, Brown, AM	P1-A4–Rear Panel Interface A10E4–Motherboard

Table 8-14. HP 83522A Cable List (Sheet 2 of 2)

Cable	Description	Connections
W21	Cable Assembly, Coax, Orange, VTUNE	P1-A1–Rear Panel Interface A10E5–Motherboard
W22	Cable Assembly, Coax, Violet, PULSE IN	J5–Rear Panel BNC (PULSE IN) A10E6–Motherboard
W23	Cable Assembly, Coax, Yellow, EXT MKR	J3–Rear Panel BNC (EXT MKR) W7J1–Shield Cage
W24	Not Assigned	
W25	Cable Assembly, Rigid, RF	A17–Modulator/Mixer A14–Amplifier (0.01 to 2.4 GHz)
W26	Not Assigned	
W27	Not Assigned	
W28	Cable Assembly, Rigid, RF	A16–Cavity Oscillator A17–Modulator/Mixer
W29	Not Assigned	
W30	Not Assigned	
W31	Cable Assembly, Power Supply	P1–Rear Panel Interface A10J3–Motherboard
W32	Cable Assembly, Ribbon	P2–Rear Panel Interface A3J1–Digital Interface Board A10J2–Motherboard J4–Rear Panel BNC (1V/GHz Output)
W33	Cable Assembly, Rigid, RF (Opt. 002)	A19–RF Step Attenuator J1–Front Panel RF OUTPUT (Type N)
W34	Not Assigned	
W35	Not Assigned	
W36	Not Assigned	
W37	Cable Assembly, Rigid, RF (Opt. 004)	DC1–Directional Detector J1–Rear Panel RF OUTPUT (Type N)
W38	Cable Assembly, Rigid, RF (Opt. 002)	DC1–Directional Detector A19–Step Attenuator
W39	Cable Assembly, Rigid, RF (Opt. 002, 004)	A19–Step Attenuator J1–Rear Panel RF OUTPUT (Type N)
W40	Cable Assembly, Rigid, RF	A12–YO A17–Modulator/Mixer

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Telex: 340192 ASC CK
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...sical Ltda
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Casilla 16475
SANTIAGO 9
Tel: 222-0282
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CM,E,M

Metrolab S.A.
Monjitas 454 of. 20E
SANTIAGO
Tel: 395752, 398296
Telex: 340866 METLAB CK
A

Olympia (Chile) Ltda.
Av. Rodrigo de Araya 1045
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SANTIAGO 21
Tel: 225-5044
Telex: 340892 OLYMP
Cable: Olympiachile Santiagochile
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China Hewlett-Packard, Ltd.
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COLOMBIA

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Telex: 44490 INST CO
Cable: AARIS Bogota
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A

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P

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Telex: 0845-430
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A,C,CM,E

Blue Star Ltd.
Band Box House
Prabhadevi
BOMBAY 400 025
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Telex: 011-71051
Cable: BLUESTAR
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Blue Star Ltd.
Sahas
414/2 Vir Savarkar Marg
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Cable: FROSTBLUE
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Blue Star Ltd.
Kalpana, 19 Vishwas Colony
Alkapuri, **BARODA**, 390 005
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Telex: 041-379
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Blue Star Ltd.
13 Community Center
New Friends Colony
NEW DELHI 110 065
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Telex: 031-61120
Cable: BLUEFROST
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Blue Star Ltd.
15/16 C Wellesley Rd.
PUNE 411 011
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Cable: BLUE STAR
A

Blue Star Ltd.
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SECUNDERABAD 500 003
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Telex: 0155645
Cable: BLUEFROST
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Blue Star Ltd.
T.C. 7/603 Poojappura
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Tel: 65799, 65820
Telex: 0884-259
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BERCA Indonesia P.T.
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P.O. Box 2497/Jkt.
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67060
TEL-AVIV
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C,M

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Via Emilia, 51/C
I-40011 **BOLOGNA** Arcola Dell'Emilia
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I-20063 **CERNUSCO SUL NAVIGLIO**
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Hewlett-Packard Italiana S p A
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Tel (045) 312-1252
C,E

JORDAN

Scientific and Medical Supplies Co
P O Box 1387
AMMAN
Tel 24907, 39907
Telex 21456 SASCO JO
C,E,M,P

KENYA

ADCOM Ltd., Inc. Kenya
P O Box 30070
NAIROBI
Tel 331955
Telex 22639
E M

KOREA

Samsung Hewlett-Packard Co. Ltd
Dongjang Yeoeuido Building
12-16th Floors
36-1 Yeoeuido-dong
Yongdeungpo-ku
SEOUL
Tel 784-2665, 784-4666
Telex 25166 SAMSAN K
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Young In Scientific Co. Ltd
Youngwha Building
547 Shinsa Dong Kangnam-ku
SEOUL 135
Tel 5467711
Telex K23457 GINSCO
A

KUWAIT

Al-Khaldiya Trading & Contracting
P O Box 830
SAFAT
Tel. 424910, 411726
Telex 22481 AREEG KT
Cable VISCOUNT
E,M,A

Gulf Computing Systems
P O Box 25125
SAFAT
Tel 435969
Telex 23548
P

Photo & Cine Equipment
P O Box 270
SAFAT
Tel 244511
Telex 22247 MATIN KT
Cable MATIN KUWAIT
P

W.J. Towell Computer Services
P O Box 5897
SAFAT
Tel 2462840
Telex 30338 TOWELL KT
C

LEBANON

Computer Information Systems S A L
Chamma Building
P O Box 11-6274 Doka
BEIRUT
Tel 69 40 73
Telex 42309
C E,M,P

LIBERIA

Unichemicals Inc
P O Box 4509
MONROVIA
Tel 224282
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P

MADAGASCAR

Technique et Precision
12, rue de Nice
P O Box 1227
101 **ANTANANARIVO**
Tel 22090
Telex 22255
P

LUXEMBOURG

Hewlett-Packard Belgium S A/N V
Blvd de la Woluwe 100
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B-1200 **BRUSSELS**
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Telex 23-494 paloben bru
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Hewlett-Packard Sales (Malaysia) Sdn Bhd
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Protel Engineering
P O Box 1917
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23½ Pending Road
Kuching, **SARAWAK**
Tel 36299
Telex 70904 PROMAL MA
Cable PROTELENG
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MRIEHEL
Tel 447 47, 455 66
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Hewlett-Packard de Mexico, S.A.
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E

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Suhail & Saud Bahwan
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Intac LLC
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Calle Samuel Lewis, Ed. Alfa
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PERU

Cia. Electro Medica S.A.
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Casilla 1030
LIMA 1
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Telex: Pub. Booth 25306 PEC PASIDR
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Hewlett-Packard (Schweiz) AG
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CH-4058 **BASEL**
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Case postale 365
CH-1217 **MEYRIN** 1
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Hewlett-Packard (Schweiz) AG
Allmend 2
CH-8967 **WIDEN**
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SYRIA
General Electronic Inc
Nuri Basha Ahnaf Ebn Kays Street
P.O. Box 5781
DAMASCUS
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Telex 411 215
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E

Middle East Electronics
P.O Box 2308
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THAILAND
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Telex 84439 Simonco TH
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TOGO
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Tunisie Electronique S.A.R.L
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M

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Teknim Company Ltd
Iran Caddesi No. 7
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Saniva Bilgisayar Sistemleri A.S.
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